4,340V, 40mΩcm$^2$ Normally-off 4H-SiC VJFET

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Abstract. This work reports the demonstration of a normally-off 4H-SiC double-gated, vertical junction field-effect transistor (VJFET) with implanted vertical channel without using epitaxial regrowth. With a 30 µm, 1.9x10$^{15}$ cm$^{-3}$ doped drift layer, over 4,300V VJFETs in the normally-off mode have been demonstrated with a specific on-resistance of 40 mΩcm$^2$ up to a drain current density of 20A/cm$^2$ at 4.5V gate bias.

Introduction

Significant progress has been made in the development of power SiC MOSFETs. However, the inversion channel carrier mobility still requires substantial improvement. Besides, the reliability of MOS-gate under high temperature and high electric field could be a major challenge. Therefore, SiC JFET, being free of gate oxide, may be an excellent candidate for high temperature and high power switching applications. A few types of vertical JFETs (VJFETs) have been reported [1-5]. To make VJFETs normally-off, one can use a buried p layer to form a low voltage, normally-off lateral JFET to control a monolithically merged normally-on vertical JFET formed by ion implantation without epitaxial regrowth [1,2] or by epitaxial regrowth [3,4]. Epitaxial regrowth, however, is costly and is less desirable. In this paper, we report the design, fabrication and characterization of a double-gated, normally-off 4H-SiC VJFET without using epitaxial regrowth.

Design and Development of Processing Technology

The cross sectional view of the VJFET is shown in Fig.1 where the n$^-$ drift layer is 30µm and doped to 1.9x10$^{15}$ cm$^{-3}$. The design of the device involves the optimization of a set of parameters including the LJFET horizontal channel opening $W_{hc}$ defined by C plus Al co-implantation, buried p layer thickness and doping concentration, and vertical trench dimensions and implantation condition. Fig.2 shows Al concentration profiles under the LJFET p$^+$ gate determined by SIMS,
which define the LJFET channel opening Whc, a key parameter for realizing normally-off VJFETs.

Fig. 3 shows the VJFET blocking characteristics for a design which results in $V_{B} = 3.559\text{V}$, simulated with ISE-TCAD [6]. Computer simulation with ISE-TCAD software was performed for VJFET structure in order to find optimum range for LJFET channel opening. Fig. 4 shows the effect of LJFET channel opening on device current density: Fig. 4a shows that channel opening smaller than 0.15$\mu$m significantly limits forward current density, while channel opening wider than 0.32mm results in a large leakage current density in normally-off blocking mode (Fig. 4b). The VJFET fabrication involves four critical implantation steps, beginning with aluminum implantation to connect the buried p layer to the wafer surface, followed by nitrogen source implantation and p$^+$ upper gate formation by Al+C co-implantation. The final one is for the vertical channel formation by nitrogen implantation, converting the buried epitaxial p layer into n$^+ \times 10^{17}$ cm$^{-3}$ doped vertical channel. Implantation masks are made of electron-beam cured photoresist for all the implantations except for the high dose Al+C co-implantation, for which Mo implantation mask is used. Post-implantation annealing of all implants is done at 1,550°C for 30 min in a controlled ambient. Multi-step junction termination extension (MJTE) with 50$\mu$m wide steps (Fig.1) is formed by ICP etching. The structure was first optimized on control diodes, which reached breakdown voltage over 5kV, and then reproduced on VJFET devices. Etched depth for the innermost MJTE step is about 1.1$\mu$m, etched depth for the outermost step is about 1.15$\mu$m, and, final isolation etching between devices is 2.85$\mu$m deep (all depths are measured with respect to the surface of the original wafer). Deep etching requires Ni and Ti-Al alloy metal masks, while shallow etching is performed with photoresist etching masks. Vertical trench is etched by ICP through nitrogen-implanted region. Etching mask is made of 0.2$\mu$m Al-Ti alloy patterned by wet etching. Additional 0.4$\mu$m Ni layer, also patterned by wet etching, protected most of the device active area during trench etching. Surface passivation is done by thermal oxide plus PECVD silicon dioxide and silicon nitride with a total thickness of about 0.85$\mu$m. Sputtered Ni/TiW annealed at 1,050°C for 10min is used for both source and gate ohmic contacts. Backside drain ohmic contact is formed by sputtered Al/Ni annealed together with source and gate contacts. Arrays of implanted upper p$^+$ gates are connected to metallized gate buses at selected locations, which results in a lower voltage across the p$^+$n gate-source junction than the externally applied gate voltage. Fig. 5 shows a microphotograph of a VJFET after all implantation steps have been completed, showing the clear formation of the upper p$^+$ gate, the vertical channel, the n$^+$ source, and the MJTE region. Fig. 6
shows the detailed features of a VJFET revealing the source and gate contact schemes and overlay formation. 4H-SiC VJFETs have been designed with active areas up to 2mm x 0.666mm.

**Evaluation and Characterization**

Fig. 7 shows the gate-to-source p+n junction I-V characteristics for a VJFET with a medium channel opening which confirms the realization of a low leakage p+n gate junction based on high dose implantation of C plus Al. The gate leakage current was seen to be only 0.4nA at a reverse bias voltage of 5V. The forward current shows some recombination current at the range of lower forward biases suggesting the need to further improve the gate processing conditions. Device characteristics above 3,000V have been measured for some of the devices under gate bias of 0V. Devices were found to be capable of blocking voltages in the range 3.0-4.3kV with the leakage current of a few milliamperes, depending on the size of the devices. Fig.8 shows the DC I-V characteristics for a large VJFET with narrow LJFET channel opening. The leakage current is 4.8mA at $V_{B}=3.056V$. Based on Fig.8, it is seen that the current density $J_D= 21.3$ and 23.8 A/cm$^2$ at $V_D=1V$ and $V_G=3.0$ and 3.5V, corresponding to $R_{SP_{ON}}$ of 47 and
The gate currents for the corresponding gate voltages are shown in the figure. One of the small VJFETs has been measured to a higher voltage of 4,340V at \( V_G = 0V \) with a leakage current \( I_D = 7mA \). Fig. 9 shows the DC I-V characteristics of the small normally-off VJFET. The gate currents at \( V_D = 5V \) are 98\( \mu \)A, 2.7mA, 12mA, 29mA and 52mA at \( V_G = 2.5V, 3.0V, 3.5V, 4.0V \) and \( 4.5V \), respectively. The forward voltage drop \( V_D \) is 0.8 V at \( J_D = 20A/cm^2 \) at \( V_G = 4.5V \). The \( R_{SP\_ON} \) is 40 m\( \Omega \)cm\(^2\) at \( J_D = 20A/cm^2 \) at \( V_G = 4.5V \) which yields a value of figure-of-merit (FOM) of \( V_B^2 / R_{SP\_ON} \) of 471MW/cm\(^2\). Forward current is also characterized at 150\(^\circ\)C for the same small VJFET under same gate voltages, and is plotted in Fig. 9 with dotted lines. In order to determine electron mobility along the current conduction path in the VJFET, simulation with ISE-TCAD was performed to fit experimental I-V curves of a selected VJFET. Electron mobility was one of the variable parameters in the simulation, and it was found to be 176 cm\(^2\)/V\( \cdot \)s for the LJFET channel and 117 cm\(^2\)/V\( \cdot \)s for the vertical channel.

**Summary**

4H-SiC VJFET has been designed and fabricated. Blocking voltage of 4.3kV is demonstrated in normally-off mode based on 30\( \mu \)m drift layer doped to 1.9\times 10^{15} \text{cm}^{-3}. Specific on-resistance of 40 m\( \Omega \)cm\(^2\) up to a drain current density of 20A/cm\(^2\) is demonstrated at \( V_G = 4.5V \), which is lower than previous world record of 69 m\( \Omega \)cm\(^2\) for VJFETs of similar (5kV) blocking voltage [4]. Electron mobility for the lateral and vertical channels are found to be 176 cm\(^2\)/V\( \cdot \)s and 117 cm\(^2\)/V\( \cdot \)s, respectively.

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**References**