1,530V, 17.5 mΩcm² Normally-off 4H-SiC VJFET Design, Fabrication and Characterization

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Abstract. This paper reports the design, fabrication and characterization of a double-gated, normally-off 4H-SiC VJFETs with implanted vertical channel, which eliminates the need of epitaxial re-growth in the middle of the device fabrication. A normally-off VJFET, which is based on a 15μm n-type drift layer doped to n=5.7×10¹⁵ cm⁻³, is demonstrated with a blocking voltage (V_B) of 1,530V with a leakage current of 15mA. The specific on-resistance (R_{SP,ON}) is found to be 17.5 mΩcm² at J_D=100A/cm² and V_G=3.5V. The VJFET conducts a drain current of 1.13A (227A/cm²) at V_G=3.5V and V_D=5V with a corresponding gate current of 16mA, resulting in an I_D/I_G ratio of 70. VJFETs with different lateral JFET channel opening dimensions have been designed and fabricated. Detailed design, fabrication and characterization results of the VJFETs are reported, including the DC I-V relations, the effects of LIFET channel opening dimensions, the specific on-resistance, and the temperature-dependent performance.

Introduction

4H-SiC VJFETs, being free of gate-oxide related problems, have been investigated by a number of groups for possible high power and high temperature applications [1-5]. To make VJFETs normally-off, one can use a buried p layer to form a low voltage, normally-off lateral JFET to control a monolithically merged normally-on vertical JFET formed by ion implantation without epitaxial re-growth [1,2] or by epitaxial re-growth [3,4]. The best normally-off VJFET employing epitaxial re-growth has a V_B of 5.3kV and an R_{SP,ON} of 69 mΩcm² at J_D~15A/cm² and V_G=+5V, corresponding to a V_B²/R_{SP,ON} of 407 MW/cm² [4]. In this paper, we report the design and development of processing technology for the demonstration of a double-gated, normally-off 4H-SiC VJFET with V_B=1,530V and R_{SP,ON}=17.5mΩcm² at a high current density (J_D) of 100A/cm², corresponding to V_B²/R_{SP,ON} of 134 MW/cm², which compares very favorably with the value of 125MW/cm² for the best 4H-SiC MOSFET of a similar blocking voltage.

Device Design, Fabrication, and Characterization

The cross sectional view of the VJFET is shown in Fig.1, where the n- drift layer is 15μm and doped to

![Cross sectional view of the VJFET](image)
The buried p gate is 0.8\textmu m, doped to 4.5\times10^{17}\text{cm}^{-3}. The top n channel layer is 0.58\textmu m, doped to 7.9\times10^{16}\text{cm}^{-3}. VJFETs are designed with three different LJFET channel opening dimensions and two active areas (0.5mm\textsuperscript{2} and 1.33mm\textsuperscript{2}). Fig.2 shows Al concentration profiles under the LJFET p\textsuperscript{+} gate determined by SIMS, which define the LJFET channel opening, a key parameter for realizing normally-off VJFET. The fabrication starts with four consecutive ion implantations: deep aluminum implantation to form a connection between buried p layer and the wafer surface at a certain region within device unit cell, shallow nitrogen implantation for the source, shallow carbon and aluminum co-implantation for the upper p\textsuperscript{+} gate, and deep nitrogen implantation to form an n-type (~7\times10^{17}\text{cm}^{-3}) conductive channel through buried p layer. Post-implantation annealing of all implants is done at 1,550°C for 30 min in argon ambient. Multi-step junction termination extension (MJTE) with a step width of 50 \mu m is formed by Inductively Coupled Plasma (ICP) etching. MJTE structure was optimized on test pn-diodes, as shown in Fig.3, which resulted in a $V_B$ over 2.3kV. In order to improve the blocking characteristics, a trench is created by ICP in the middle of the implanted n-type vertical channel. Surface passivation is done by thermal oxidation at 1100°C for 3 hours in wet oxygen, followed by deposition of 600nm- thick PECVD silicon dioxide and 200nm- thick PECVD silicon nitride. The windows for Ohmic contacts are opened in the passivation layer by a combination of ICP etching and wet etching with buffered oxide etch (BOE). Gate and

Fig.2 Al concentration profiles under the LJFET P\textsuperscript{+} gate.

Fig.3 Test results of MJTE.

Fig.4 Gate-to-source p\textsuperscript{+}n junction I-V curve.
source Ohmic contacts are formed with sputtered Ni/TiW (20/80 nm). Drain contact is formed with sputtered Al/Ni (20/300 nm) on the substrate. All contacts were annealed simultaneously at 1,050°C for 10 min. Ti/Au is used to form overlay buses and bonding pads. Total overlay thickness is 1.7 μm for the source and 0.8 μm for the gate. Arrays of the implanted upper p+ gates are connected to metallized gate buses at selected locations, which results in a lower voltage drop across the p+n junction gate than the externally applied gate voltage. Fig.4 shows the gate-to-source p+n junction I-V characteristics and Fig.5 presents the gate-to-drain p-n I-V curve for a VJFET with wide LJFET channel opening. The results confirm the realization of a good p+n gate junction based on high dose implantation of C plus Al. Fig.6 shows the DC I-V & J-V characteristics of a small VJFET (active area 0.5mm²) with wide LJFET channel opening. Forward current is characterized at both room temperature and 150°C. At room temperature, the leakage current is 15mA at Vb=1,530V. Based on Fig.6, it is seen that, at VG=3.5V, the current density JD is 50 and 100 A/cm² at VD=0.84V and 1.75V, respectively, corresponding to an RSP,ON of 16.8 and 17.5 mΩcm², respectively. At room temperature, the gate currents are 94μA, 2.7mA, 16mA and 43mA for VG=2.5, 3, 3.5, and 4V, respectively. RSP,ON of 16.8 and 17.5 mΩcm² and Vb of 1,530V correspond to a figure-of-merit (FOM) of Vb²/RS,ON of 139 and 134 MW/cm², respectively. As a reference, the best 4H-SiC UMSFET with a similar voltage rating has a Vb²/RS,ON of ~125 MW/cm² [6]. Fig. 7 shows the DC I-V & J-V characteristics of a large VJFET (active area of 1.33mm²) with wide LJFET channel opening. For 3.5 V gate bias, the specific on-resistance corresponding to JD = 50 and 100 A/cm², is 21.6 and 25.8 mΩcm², respectively. Fig. 8 shows the DC I-V & J-V characteristics of a small VJFET with narrow LJFET channel opening. As could be seen by comparing to Figs. 6 and 7, the VJFET with narrow LJFET channel opening requires higher gate bias for device to conduct appreciable amount of current (1.5V compared to 1.0V for wide LJFET channel opening). For 3.5 V gate bias, the specific on-resistance corresponding to JD of 50 and 100 A/cm², is 18.8 and 21.4 mΩcm², respectively. At room temperature, the gate currents are 270μA, 18mA, 75mA and >100mA for VG=2.5, 3, 3.5, and 4V, respectively. As could be noticed, devices with wider LJFET channel opening (lower dose and shallower p+ Al+C co-implantation) demonstrate lower gate current under same gate-to-source and
drain-to-source biases. The ratio of drain current to gate current under same bias conditions is higher for devices with wider LJFET opening. Leakage current in blocking mode under zero gate bias depends not only on LJFET channel opening, but also on the structure of the vertical channel.

**Summary**

A double-gated 1.53-kV normally-off 4H-SiC VJFET with implanted vertical channel has been demonstrated. A low specific on-resistance $R_{SP,ON}$ of 17.5 m$\Omega$cm$^2$ has been achieved, resulting in a FOM of $V_B^2/R_{SP,ON}$ of 134 MW/cm$^2$, which is larger than 125 MW/cm$^2$ of the best reported 4H-SiC MOSFET [6]. This VJFET approach is attractive because it does not require expensive epitaxial regrowth in the middle of the fabrication process. The existing device structure and fabrication process may be applied to achieve higher blocking voltages, which will require modifications to the wafer structure (mainly n-type drift and p-type buried layers).

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**References**