A High Voltage (1570V) 4H-SiC Bipolar Darlington with Current Gain \( \beta \geq 640 \) and Tested in a Half-bridge Inverter up to 20A at \( V_{\text{Bus}}=900V \)

J. H. Zhao\(^1\), J. Zhang\(^1\), P. Alexandrov\(^2\), and T. Burke\(^3\)

1. SiCLAB, ECE Dept., Rutgers University, 94 Brett Road, Piscataway, NJ 08854, USA
2. United Silicon Carbide, Inc., Building A, 100 Jersey Ave, New Brunswick, NJ08901, USA
3. US Army TACOM, Warren, MI 48397-5000

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**Abstract.** This paper reports the design, fabrication and characterization of a 4H-SiC bipolar Darlington transistor with both high common emitter current gain and high blocking voltage. The driving and output transistors were and fabricated on the same chip with a 12\( \mu \)m, 8.5\( \times \)10\(^{15} \)cm\(^{-3} \) doped drift layer. The Darlington’s driving transistor was capable of 1,600V and 5.3A with a maximum DC current gain \( \beta_1=26 \) at a collector current \( I_{C1}=3.12A \) (\( I_{C1}=260A/cm^2 \)) and \( V_{CE1}=4.2V \), and a specific on-resistance (\( R_{SP,ON} \)) of 12.2m\( \Omega \)cm\(^2 \) for currents up to \( I_{C1}=3.65A \) (\( I_{C1}=304A/cm^2 \)) and \( V_{CE1}=3.7V \). The output transistor can handle over 23A and a blocking voltage higher than 1600V with a peak DC current gain \( \beta_2=22.3 \) at \( I_{C2}=15.7A \) (\( I_{C2}=262A/cm^2 \)) and \( V_{CE2}=4.54V \), and an \( R_{SP,ON} \) of 16.7m\( \Omega \)cm\(^2 \) for currents up to \( I_{C2}=18A \) (\( I_{C2}=300A/cm^2 \)) and \( V_{CE2}=4.1V \). The maximum AC current gain of the hybrid BJT Darlington at room temperature was \( \beta \geq 640 \). The DC current gain at room temperature was found to increase with the collector current, up to 462 at \( I_C=13.9A \) (\( I_{C2}=232A/cm^2 \)) and \( V_{CE2}=10.6V \), limited only by the measurement instrument. The Darlington can block voltages up to 1571V, conduct an \( I_C \) of 14A at \( V_F=7.7V \) and has a differential \( R_{SP,ON} \) of 16.7m\( \Omega \)cm\(^2 \) at \( J_{C2} \) up to over 240A/cm\(^2 \) (\( I_C=14.4A \)). Inductively-loaded half-bridge inverter switching is also reported at 900V-20A.

**Introduction**

Due to its excellent material properties of high critical field and wide bandgap, 4H-SiC has been widely investigated for high temperature and high power applications. 4H-SiC power bipolar junction transistors (BJTs) are gaining increased attention in recent years partly because BJTs are free of gate oxide problems and have the potential to achieve low on-state voltage at high current density\([1-5]\). The main disadvantage of SiC BJTs, however, is the low current gain or the high base driving current requirement. Darlington transistor can drastically reduce the base current requirement but at the expense of increased forward voltage drop (\( V_F \)), making Darlington transistors attractive only at a relatively high voltage region. Among the best results of earlier efforts are (i) a monolithic 4H-SiC Darlington of \( I_C=0.3A \) at \( V_{CE}=7.5V \) with a corresponding DC current gain \( \beta \geq 40 \) at \( J_C \geq 50A/cm^2 \) \([6]\), (ii) a hybrid Darlington of 500V, >200A/cm\(^2 \) (>23A) at \( V_{CE}=6.4V \) with a DC current gain of 430 at \( J_C \approx 200A/cm^2 \) \([7]\), and (iii) a hybrid Darlington of 3.9A(278A/cm\(^2 \)) at \( V_{CE}=6.3V \) with a maximum AC current gain of 500 and an estimated DC current gain of 367\([8]\). This paper reports a 4H-SiC high power(1,570V-14A) hybrid Darlington with an AC current gain of 640 and a DC current gain \( \beta \geq 462 \) (limited by measurement instrument).

**Design and Fabrication**

The 4H-SiC BJT driving transistor (active area=1.2mm\(^2 \)) and output transistors (active area=6.0 mm\(^2 \)) were fabricated on the same chip. The 4H-SiC wafer was purchased from Cree Inc. The emitter n-type epi-layer is 0.8\( \mu \)m, doped to \( 2 \times 10^{19} \) cm\(^{-3} \). The base is a 1.0\( \mu \)m p-type epi-layer with a
doping concentration of $4.1 \times 10^{17}$ cm$^{-3}$. The collector is formed by a 12µm drift layer with n-type doping of $8.5 \times 10^{15}$ cm$^{-3}$ and the n$^+$-type 4H-SiC substrate. The emitter mesa depth was 0.93µm, defined by inductively coupled plasma (ICP) etching. The base contact region was implanted by carbon and aluminum co-implantation at room temperature which consists of C ions of $4 \times 10^{14}$ cm$^{-2}$ at 28keV, $5.2 \times 10^{14}$ cm$^{-2}$ at 60 keV, and $1.1 \times 10^{14}$ cm$^{-2}$ at 75 keV plus Al ions of $3.6 \times 10^{14}$ cm$^{-2}$ at 50 keV and $7.5 \times 10^{14}$ cm$^{-2}$ at 100 keV. The designed spacing between the base implanted region and the emitter edge is 3µm. Post-implantation annealing was done at 1550°C for 30 minutes in Ar. The devices were isolated by a mesa etching of ~1.4µm into the drift layer. The passivation was done first by a 2-hour wet thermal oxidation at 1100°C, followed by a 1-hour Ar annealing at 1100°C. The sample was then annealed for 3 hours at 950°C for the low-temperature wet-oxygen re-oxidation. After the thermal oxidation, 250nm SiO$_2$ and 250nm Si$_3$N$_4$ were deposited using PEVCD to increase the passivation layer thickness. Both emitter and base contact metal was 200nm Ti covered by 200nm TiN. This Al-free Ohmic contact eliminated the possible Al-spiking during the following high temperature Ohmic contact annealing.

![Fig.1. Formation of a Darlington transistor.](image1)

![Fig.2. I-V characteristics of the driver BJT.](image2)

![Fig.3. I-V characteristics of the output BJTs.](image3)

![Fig.4. I-V characteristics of the Darlington at room temperature.](image4)

![Fig.5. I-V characteristics of the Darlington at 150°C.](image5)
ALTi(20nm)\Ni(700nm) bi-layer was used as the collector contact metal on the substrate. All the contacts were annealed in hydrogen and nitrogen forming gas for 8 minutes at 1050°C. After the ohmic contact formation, another layer of PECVD SiO₂ (410nm) and Si₃N₄ (250nm) was deposited for insulation between the overlay metals. Finally the overlay metals of Ti(50nm) and Au(1.5μm) were deposited to connect emitter fingers and to form base and emitter bonding pads.

A hybrid Darlington was formed by packaging a single chip containing six high voltage BJT cells with one serving as the driving transistor(T1) and the rest of the five paralleled BJT cells serving as the output transistor(T2). As shown in Fig.1, the emitter pin of the driving transistor was connected to the base pin of the output transistor, which leads to the single-chip hybrid Darlington with a DC current gain $\beta$=$\beta_1+\beta_2+\beta_1\times\beta_2$ where $\beta_1$ and $\beta_2$ are the DC current gain of the driving and output transistors, respectively.

Characterization and Discussion

The fabricated 4H-SiC bipolar Darlington transistor was characterized by using Tektronix 371A curve tracer, Keithley 248 high voltage source and Keithley 6517A electrometer. Fig.2 shows the I-V characteristics of the driving BJT at room temperature and 150°C. The peak DC current gain was 26 at $I_{C1}$=3.12A ($J_{C1}$=260A/cm²) and $V_{CE1}$=4.2V at room temperature with an $R_{SP,ON}$ of 12.2mΩ cm² at collector currents up to $I_{C1}$=3.65A ($J_{C1}$=304A/cm²) and $V_{CE1}$=3.7V. Fig.3 shows the I-V characteristics of the output transistor at room temperature and 150°C with a peak DC current gain of 22.3 at $I_{C2}$=15.6A ($J_{C2}$=260A/cm²) and $V_{CE2}$=4.5V with an $R_{SP,ON}$ of 13.4mΩ cm² for currents up to $I_{C2}$=18A ($J_{C2}$=300A/cm²) and $V_{CE2}$=4.1V. The negative $I_C$--$V_{CE}$ slope in the active region as shown in the room-temperature I-V curves in Fig.2 and Fig.3 is mainly due to self-heating that is aggravated by current crowding.

The hybrid Darlington I-V characteristics at RT is shown in Fig.4. The entire hybrid Darlington transistor was measured up to $I_C$=14A and $V_{CEO}$=1571V with a leakage current of 0.26mA, representing the highest power for SiC bipolar Darlington transistors reported to date. The maximum AC current gain was >640. The maximum DC current gain of 462 was obtained at $I_C$=13.9A ($J_{C2}$=232A/cm²) and $V_{CE}=10.6V$ at room temperature, limited only by the measurement set-up. The trade-off is an on-set voltage of 3.3V determined from a linear extrapolation of the I-V curve in the saturation region shown in Fig.4. The differential $R_{SP,ON}$ of the Darlington was 16.7mΩ cm² for $J_{C2}$ up to over 240A/cm² ($I_C$=14.4A). The Darlington I-V characteristics at 150°C is shown in Fig.5. The Darlington current has been measured to more than 5A at 150°C, limited again by the measurement set-up. The Darlington shows an AC current gain of 248 and a DC current gain of 145 at 150°C, and an $R_{SP,ON}=34.7$mΩ cm².

![Graphs](image.png)

Fig.6. DC current gain versus collector current and current density.
Fig. 6 shows the DC current gain versus the collector current density at Vce=10V for the driving BJT(T1), the output transistor(T2) and the BJT Darlington transistor respectively, both at room temperature and 150°C. A simple examination confirms that the experimental results of Fig.6(a), (b) and (c) are, as expected, in a good agreement with the expression of $\beta = \beta_1 + \beta_2 + \beta_1 \times \beta_2$.

The packaged 4H-SiC Darlington transistor has been tested in an inductively-loaded(1mH) half-bridge inverter circuit at a bus voltage of 900V and a switching current of 20A. 4H-SiC MPS (Merged-PiN-Schottky) diodes were used as the free-wheeling diodes. Fig.7 shows the switching waveforms. This is the highest switching voltage reported to date for SiC BJT inverters. The collector current rise time was 0.10μs and the fall time was 0.32μs. The turn-on switching energy loss was 9.85mJ, and the turn-off switching loss was 3.16mJ. The $V_{CE,ON}$ was 12V when the base driving current was around 100mA, corresponding to an operation point at the edge of the saturation region and the active region with a current gain of 200. Before the BJT Darlington entered the saturation region, the base current was around 50mA, corresponding to a current gain of 400.

**Summary**

A high current gain($\beta > 640$) and high power(1571V-14A) 4H-SiC hybrid Darlington BJT was demonstrated, showing a differential $R_{SP,ON} = 16.7\ \text{mΩ cm}^2$ up to $J_{CE} = 240\ \text{A cm}^2$. The hybrid Darlington transistor has been tested in an inductively-loaded half-bridge inverter at a bus voltage of 900V and a switching current of 20A. This is the highest bus voltage and power tested in an inverter for SiC BJTs or Darlington transistors.

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