Multi-Rate Filter Design

Mitch Gollub, Jay Nadkarni, Digant Patel, Sheldon Wong

{mgollub, nadkarni, dcp115, shelwong}@scarletmail.rutgers.edu

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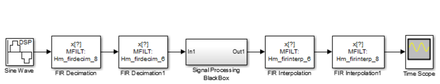
Goal

- ❑ To explore a set of reliable filter designs and construction methods for specific hardware applications
- ❑ Investigate the tradeoff between area and performance
- ❑ Understand mapping and testing of a DSP design from MATLAB to FPGA

Motivations and Objectives

To explore a set of reliable filter designs and construction methods for specific hardware applications. One specific difficulty in filter design is the climbing computational load of a high sampling rate system. Filters are commonly implemented as FIR(Finite Impulse Response) filters. At higher sampling rates, there will more data samples that need to be processed, therefore requiring a higher computational load.



Research Challenges

- ❑ Learning Digital Filter Design methods
- ❑ Using MATLAB/Simulink and LabVIEW
- ❑ Understanding Computation Benefits of Multi-Rate Filtering

Future Work

- ❑ FPGA Implementation at 44.1kHz for audio
- ❑ Effects to be built in to Filter (for lighter computation)
- ❑ Application to communications

Acknowledgement

We would like to thank **Northrop Grumman, National Instruments, Prof. Spasojevic,** and **Swapnil Mhaske.**

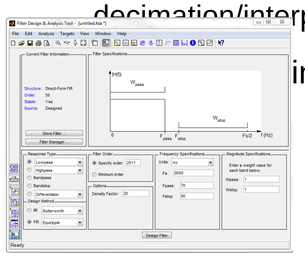
Methodology

Design Methodology

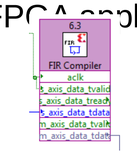
- ❑ Design a Multi-Rate Filter Bank
  - ❑ Make multi-rate filter specifications
  - ❑ Define filter order using specifications
  - ❑ Calculate coefficients (fdatool)
- ❑ Implement Filter Bank as Block Diagram in Simulink
  - ❑ Create filter objects in MATLAB
  - ❑ Design Simulink model
  - ❑ Import filter objects to model
- ❑ Run Simulations to verify design
  - ❑ Use a time scope/frequency analyzer to observe output signal
  - ❑ Redesign if results are unexpected

Implementation Methodology

- ❑ Export MATLAB generated coefficients
  - ❑ Create .coe coefficient file for Xilinx based FPGA
- ❑ Utilize .coe coefficient file in LabVIEW filter block
- ❑ Configure filter block parameters to specifications
  - ❑ Assign filter options (i.e. single rate decimation/interpolation)



into an FPGA application



Results

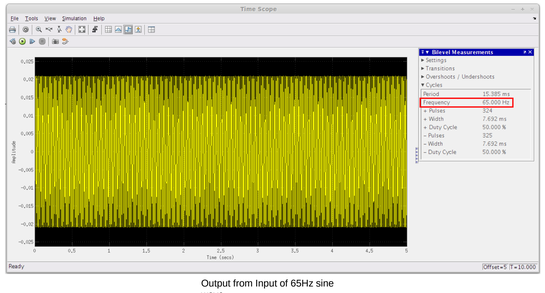
Results:

Calculations

Single Rate: 2512/2 MACs/sample * 8000 samples/sec = **10048 kMACs/sec**

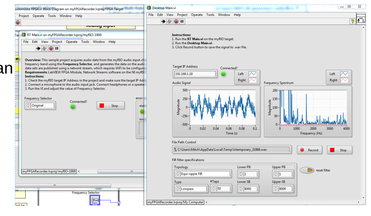
Multi Rate (8x6): ((226/2MACs/sample) * (8000 samples/sec) * (1/ 8 decimation factor)) + ((339/2MACs/sample) * (1000 samples/sec) * (1/ 6 decimation factor)) = **141kMACs/sec** (Less than ~10,000kMACs/sec Single-Rate)

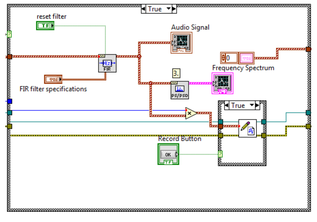
MATLAB Simulation

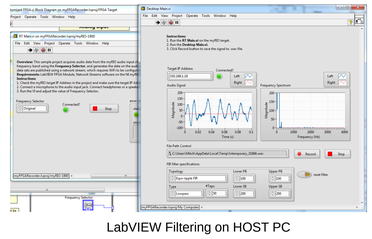


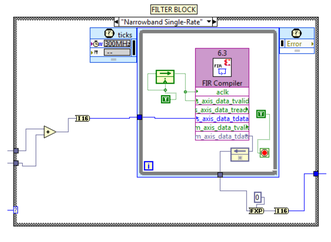
Output from Input of 65Hz sine wave

LabVIEW Filtering









LabVIEW Filtering on HOST PC

References

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[2] http://edge.rit.edu/content/P14224/public/Software/MyRIO%20Software/Control%20Software/documentation/myRIO%20Custom%20FPGA%20Project%20Documentation.html