SYLLABUS FOR INTEGRATED CIRCUIT DESIGN 588 SPRING 2014

Prof. Michael Caggiano
Office Hrs: EE 111; Monday. & Thursday. 2:00 – 3.00 PM

Reference Text: Microelectronic Circuit Design, R.C. Jaeger, T.R Blalock, 4th Ed.
Reference Text: Microelectronic Circuits, Sedra & Smith.

CHPTR		# of LCTRS
3.1-3.4 3.6 3.7	Review of RC circuits, Diodes: pn junction diode dynamics, diode switching characteristics.	3
5.5-5.6 5.8- 5.8.4 9.10	BJT Transistor: Dynamic transistor models, piecewise sequential model for switching operations. Storage time, Delay time, Rise time.	2
9.11-9.12	Logic Gate Structures Using BJT's: RTL, DTL and TTL, design parameters for TTL, switching speeds for basic TTL gates, improved recovery, high speed gates, saturation control.	3
9.1-9.7	BJT Non-saturating Gate Circuits: Direct-coupled emitter follower logic, basic form of ECL, some variations in performance and evolution of ECL.	2
4.1-4.6	FET Transistor: basic equations, characteristics, empirical models and SPICE models of the FET.	2
6.5-6.10 6.11-6.11.2	FET Logic Gate Structures: FET's as switches and active loads, switching speeds, sizing and power for NMOS gates, **Test 1 – Beginning of March**	2
7.1-7.9	Complementary FET structures, switching speeds and power for CMOS	4
8.1-8.7	CMOS Regenerative Circuits: SR latch, triggering, and logic gate flip flop circuits, JK flip flop, D flip flop, shift registers and counters, MOS static and dynamic shift registers, charge-coupled device as shift registers.CMOS ROM and RAM cells. CMOS static Ram Cells.	4
7.10, 12.6.3	Analog Signal Processing: CMOS Transmission gates, CMOS sampling circuits.	2
12.5-12.6	Digital to Analog and Analog to Digital Converters sampling rate, quantizing and digitizing, implementation and techniques.	2

Projects 25 points
Mid-Term 25 points
Final 50 points