MOSFET Based Ultra-low Power Realization of Analog Joint Source-Channel Coding

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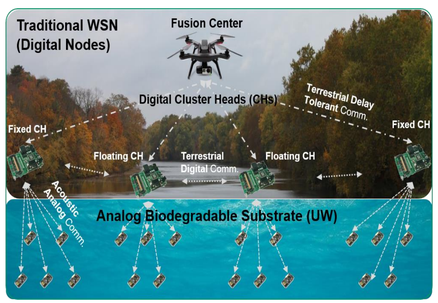
Introduction and Motivation



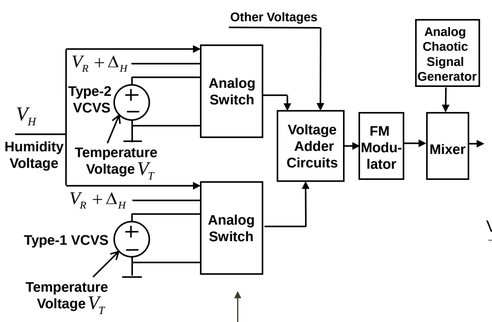
Analog Joint Source-Channel Coding (AJSCC)

- First proposed by Shannon (so called Shannon Mapping)
- Compresses two or more signals into one with controlled distortion
- No. of levels decided by Δ_H

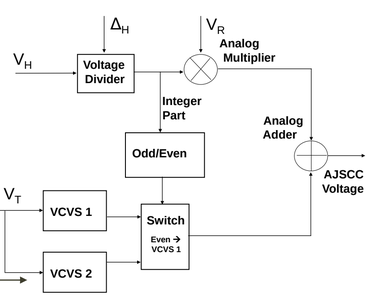
Novel Architecture for Wireless Sensor Networks [1]

- High density (spatial and temporal) and persistent sensing
- Power Consumption
  - Existing Energy Harvesting produces only tens of μW
  - Transmission using RF ~50μW, leaving only ~30μW for Encoding
  - Existing Encoding Designs: ~60μW
  - Ultra-low power possibilities with use of a MOSFET
- Applications Include:
  - Environmental monitoring
  - Infrastructure surveillance
  - Intelligent transportation systems
  - …and many more

Related Work



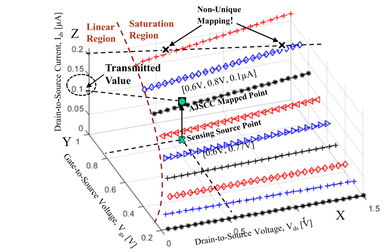
Design 1 (parallel VCVS)



Design 2 (Programmable VCVS)

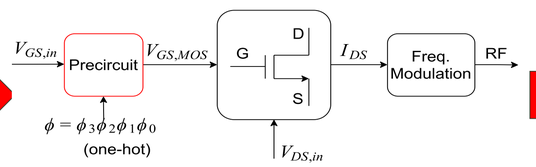
Most of the **existing** realizations of AJSCC are in **digital domain** except our previous works (Designs 1 and 2 shown here [1],[3])

Proposed Solution: MOSFET-based Realization for AJSCC

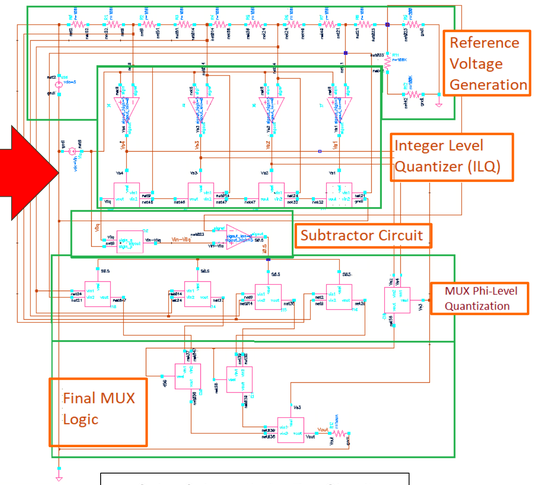


$$I_{ds} = \frac{1}{2} \cdot \frac{W}{L} \cdot \mu C_{ox} \cdot (V_{gs} - V_{th})^2 \cdot (1 + \lambda V_{ds})$$

I_{ds} vs V_{ds} for different V_{gs} of a MOSFET in Saturation Region with Channel Length Modulation (CLM). Linear Region is not shown.



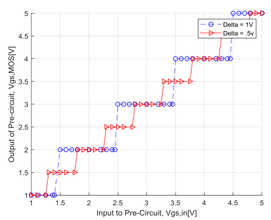
MOSFET-based encoding for AJSCC with different φ



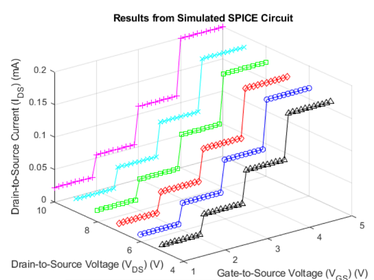
Spice Schematic for Pre-Circuit

- **Challenge**: Finding the optimized delta from only having the distribution known at the receiver
- Realization of AJSCC using I-V characteristics of a MOSFET
- **Challenge**: Non-unique mapping of two pairs of V_{gs} and V_{ds} to the same I_{ds}
- Propose a pre-circuit design to accommodate different levels of quantization (φ) in the y-axis of AJSCC

Performance Evaluation: Experimental Results: SPICE Results (Left) and Breadboard (Right)



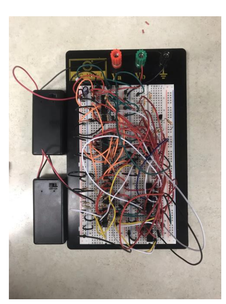
Vgs,in varied to Vgs, MOS for different φ values



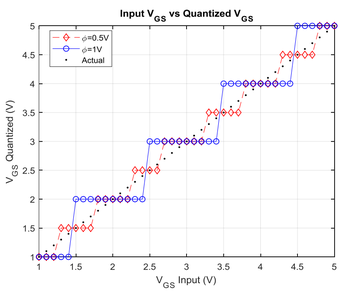
Vgs,in and Vds,in varied to Ids

Power Consumption

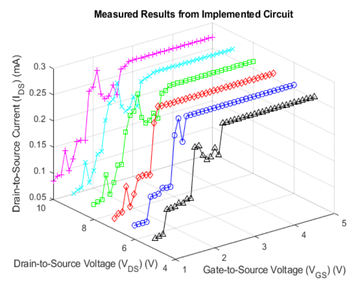
φ	Breadboard Results	SPICE Simulation	Latest IC Design
.5V	approx. 2mW (5V into 0.4mA)	approx. 0.60mW (5V into 120μA)	approx. 8μW
1V	approx. 1.5mW (5V into 0.3mA)	approx. 0.40mW (5V into 80μA)	approx. 8μW



Breadboard Implementation of Pre-Circuit



Vgs,in varied to Vgs, MOS for for different φ values



Vgs,in mapped to Vgs,MOS mapped to Ids by the pre-circuit

Discussion and Future Work

- Using the latest nm-Silicon technology, for 9 AJSCC levels (φ= 0.5 V, 2-stages), power consumption is ≈ 8μW
- Reduce the complexity of the pre-circuit by using less multiplexers
- Test design under different wireless channels

Acknowledgement

We would like to acknowledge PhD Student Vidyasagar Sadhu, as well as Dr. Dario Pompili for his assistance and guidance, Undergraduate Director Hana Godrich, with special mention to Lab Facilities Specialist Kevin Wine and Systems Administrator John Scafidi

References

[1] V. Sadhu, X. Zhao, and D. Pompili, "Energy-efficient Analog Sensing for Large-scale, High-density Persistent Wireless Monitoring," in Proc. of *IEEE Annual Conference on Wireless On-Demand Network Systems (WONS), February 2017*
[2] C. Shannon, "Communication in the Presence of Noise," *Proceedings of the IRE*, 1949
[3] X. Zhao, V. Sadhu, A. Yang, and D. Pompili, "Improved Circuit Design of Analog Joint Source Channel Coding for Low-Power and Low-Complexity Wireless Sensors," in *IEEE Sensors Journal*, vol. 18, pp. 281-289, January 2018