Goal

- Design a pipelined, RISC-V compliant, RV32I processor core
- Support arithmetic operations, memory accesses, and changing logic flow
- Implement a 5-stage, classic RISC pipelined architecture
- Include hazard detection and a stall insertion mechanism
- Build a terminal interface for output over VGA
- User input to interact with the system
- Develop applications that showcase processor capabilities
- Accelerate the advent of open source computing

Motivation and Objectives

- Motivation
  - RISC-V is a recently-introduced, modern, open-source Instruction Set Architecture (ISA)[1]
  - The RISC-V community welcomes Processor Core Implementations to help grow adoption of the ISA
- Objectives
  - Develop custom, open-source processor platform
  - Create a starting point for future related projects
  - Demonstrate the advantages of the RISC-V Platform:
    - High Efficiency | Small Size | Low Cost

Research Challenges

- Timing issues required multiple iterations of processor design and development
- Multiple references used to assist mapping out custom design of the processor[1][3]
- Some RISC-V Instruction Set extensions are in draft stage and still being developed

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Methodology

- Translated the RISC-V ISA specification into a system of components
- Processor implementation consists of Python script generated and handwritten VHDL
- Controller component determines processor operation from the current program instruction and selects the components to use
- Controller is generated using a Python script given a table of instructions and corresponding control signals
- Processor and supporting hardware designs are loaded onto a Xilinx Zynq-7000 FPGA[2] via Vivado synthesis and implementation

Results

- Demonstration programs are written in RISC-V assembly language
  - Output graphics and text to terminal
  - Games take input from user
- Unit tests written in RISC-V assembly language used to verify processor features
- Processor runs at 25MHz and uses .22W of Power

References

[1] https://riscv.org/specifications/
[3] https://riscv.org/risc-v-books/