# Configurable In-line Video Refinement (CIVR)

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CIVR

## Goal

CIVR is a project that aims to provide an efficient and inexpensive solution to real time low latency graphics processing. This presentation will highlight the problems of current graphics processing solutions and show how CIVR solves them. Additionally, this presentation will explain the design philosophy behind CIVR and why it is so efficient. Lastly, it will address the production cost of the current CIVR prototype and offer a projection of possible cost savings afforded by mass production.

## Motivations and Objectives

### Motivations

- Many modern graphics processing algorithms involve full-frame analysis and computation which requires high-overhead computations prior to displaying the display output causing lag
- Existing external boxes usually only implement a single feature each and would be extremely costly to implement all of our features

### Objectives

- Create a low latency inexpensive video refinement unit
- Incorporate many common graphics enhancements (anti-aliasing, dithering, etc.)

## Research Challenges

- DVI shield and mounting holes not to spec due to error in Molex datasheet
- Blue and green output noise due to the most significant bit data lines being too long and not arriving in time for the positive edge of pixel clock
- JTAG programmer would not detect the FPGA
- Level-shifting MOSFETs are too slow to communicate via I2C at 100 kbps to transmit and modify EDID

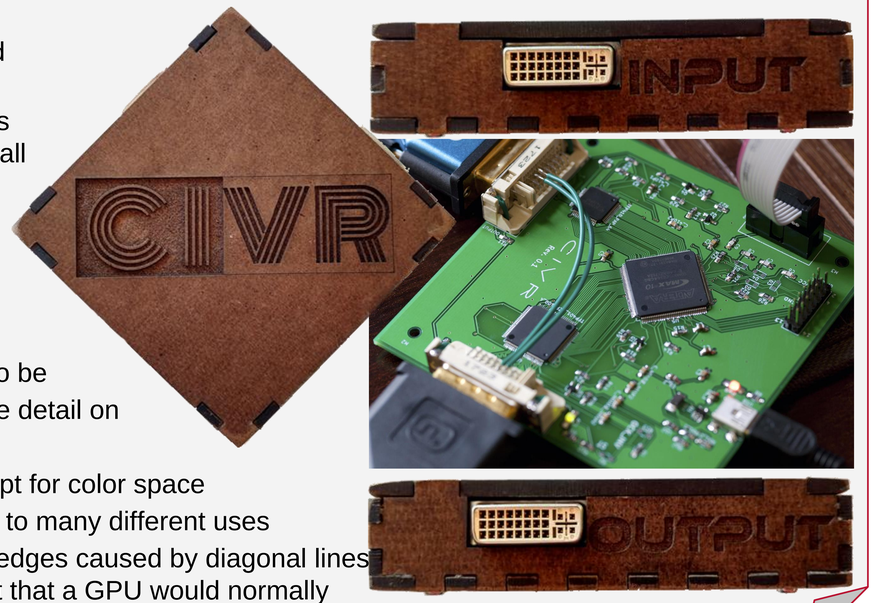
## Acknowledgement

We would like to acknowledge Professor Predrag Spasojevic for all his help and encouragement during our endeavor. We would also like to thank professor Hana Godrich and the rest of the ECE department for their resources and support

## Results

### PCB Prototype

- A PCB was fabricated and hand assembled to specifications
- The resulting PCB functioned as intended and is able to support all resolutions supported by DVI
- The cost to produce a board came out to under the targeted $35 even in a very limited run



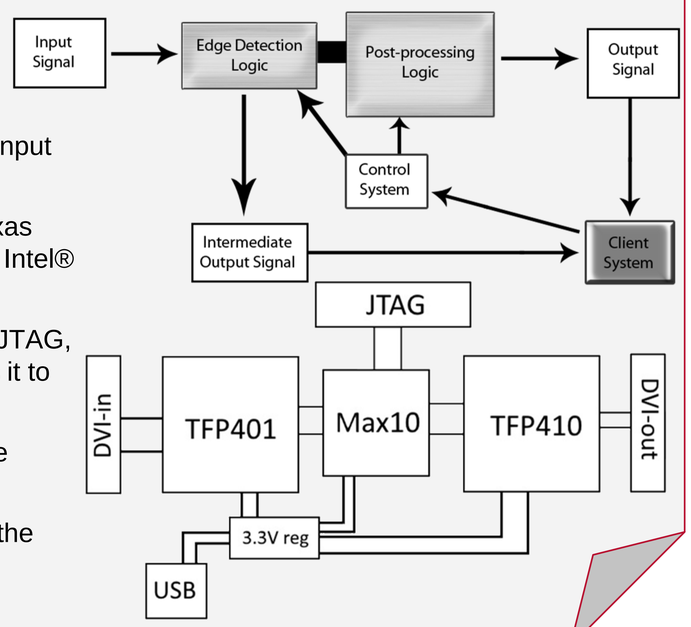

### Software

- The dithering algorithm proves to be especially useful in showing more detail on lower bit displays
- Grayscale shows proof of concept for color space conversion which can be applied to many different uses
- Anti-aliasing helps to fix jagged edges caused by diagonal lines and offloads the performance hit that a GPU would normally take in doing so

## Methodology

### Methodology

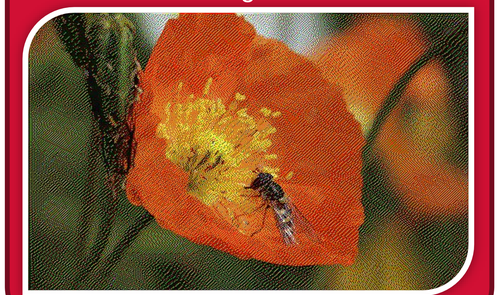
- The device is USB powered (it can also run passively via the 5 volt line of the DVI input)
- A computer sends a display signal to the DVI input of the device
- The input DVI signal is deserialized by the Texas Instruments TFP 401 and passed along to the Intel® MAX® 10 FPGA
- The Intel® MAX® 10 FPGA, programmed via JTAG, processes and modifies said signal and sends it to the Texas Instruments TFP 410
- The Texas Instruments TFP 410 serializes the modified signal and sends it to the DVI output
- The DVI output sends the enhanced signal to the displayed device




## Effect Pictures

### Dithering

1-bit Image Before



1-bit Image After

### Grayscale

Before

After

## References

[1] Max 10 Documentation https://www.altera.com/products/fpga/max-series/max-10/support.html
[2] Texas Instruments TFP401 Documentation http://www.ti.com/lit/ds/symlink/tfp401.pdf
[3] Texas Instruments TFP410 Documentation http://www.ti.com/lit/ds/symlink/tfp410.pdf

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