ECE Capstone program
Spring 2018
Summary Project info

Please provide the following information to be shared with on capstone information exchange platform:

1. Project number: S18-22

2. Project title (as will appear on the poster): RISC-V IDE SIM

3. Team members: Skyler Malinowski, Arjun Ohri, Alejandro Aguilar, Raj Balaji
4. Adviser(s) name(s): Maria Striki

5. Up to 10 keywords that will help to classify the project:
RISC-V, Computer Architecture, Assembly Language, Software, Learning, Academic, IDE, Simulator, Open source, Educational

6. Project abstract (up to 200 words) to be shared with judges:

The purpose of this project is to design and synthesize a software solution to fill the void in academic markets for a light-weight solution to computer architecture simulation. More specifically, to aid in the development and teaching of RISC-V architecture and assembly language through providing an Integrated Development Environment (IDE) equipped with useful tools – of such, a real-time code simulator is of the core feature set.

In an effort to remain relevant, the project design is one with the future in mind – employing bleeding-edge cross-platform and open-source frameworks – while staying completely open-source, itself. This way our software solution may change with the demand from consumers and community while being able to adapt to the open source nature of RISC-V architecture in by keeping a single unified codebase under a copyleft license hosted in a repository.