Signal Names and Active Levels

- Signal names are chosen to be descriptive
- Active levels -- HIGH or LOW
  - Named condition or action occurs in either the HIGH or the LOW state, according to the active-level designation in the name.

<table>
<thead>
<tr>
<th>Active Low</th>
<th>Active High</th>
</tr>
</thead>
<tbody>
<tr>
<td>READY~</td>
<td>READY+</td>
</tr>
<tr>
<td>ERROR.L</td>
<td>ERROR.H</td>
</tr>
<tr>
<td>ADDR15(L)</td>
<td>ADDR15(H)</td>
</tr>
<tr>
<td>RESET*</td>
<td>RESET</td>
</tr>
<tr>
<td>ENABLE~</td>
<td>ENABLE</td>
</tr>
<tr>
<td>~GO</td>
<td>GO</td>
</tr>
<tr>
<td>/RECEIVE</td>
<td>RECEIVE</td>
</tr>
<tr>
<td>TRANSMIT_L</td>
<td>TRANSMIT</td>
</tr>
</tbody>
</table>

we will use this notation ➔
Errors and Active Levels

- Logic Circuit: HIGH when error occurs
- Logic Circuit: LOW when error occurs
- Error Levels:
  - ERROR
  - ERROR_L
  - ERROR1_L

Flat Schematic Structure
Buffer

- A buffer is a gate with the function $F = X$:

$$X \rightarrow F$$

- In terms of Boolean function, a buffer is the same as a wire connection!
- So why use it?
  - A buffer is an electronic amplifier used to improve circuit voltage levels and increase the speed of circuit operation.
**Gate Symbols [recall Lecture #4]**

- $X + Y$  
- $(X + Y)'$  
- $X \cdot Y$  
- $(X \cdot Y)'$  
- $X$  
- $X'$  

**OR**  
**NOR**  
**AND**  
**NAND**  
**BUFFER**  
**INVERTER**

---

**DeMorgan Equivalent Symbols [Lecture #4]**

- $X + Y$  
- $(X + Y)'$  
- $X \cdot Y$  
- $(X \cdot Y)'$  
- $X$  
- $X'$  

**OR**  
**NOR**  
**AND**  
**NAND**  
**BUFFER**  
**INVERTER**

- “bubble-to-bubble design”

- Which symbol to use?  
- Answer depends on signal names and active levels
Example Schematic

\[ X = A_L \cdot B + A \cdot B_L \]

\[ Y = A_L \cdot C + B \cdot C \]

HCT = high-speed CMOS
TTL compatible

Circuit Timing

Causality and propagation delay:
- GO
- READY
- DAT
- ENB (enable) is constant
- \( t_{PD} \)
- \( t_{c} \)
- \( t_{min} \)
- \( t_{max} \)
- Shorter
- Longer

Minimum and maximum delays:
- Go
- Ready
- Dat
- ENB
- \( t_{PD} \)
- \( t_{c} \)
- \( t_{min} \)
- \( t_{max} \)

Another graph for the ENB input ...
### Timing Diagrams for “Data” Signals

**Certain and uncertain transitions:**

- **WRITE L:** write is on “0”
- **DATA IN:** must be stable
- **DATA OUT:** old data must be stable then new data

**Sequences of values on an 8-bit bus:**

- **CLEAR**
- **COUNT**
- **STEP[7:0]**
  - FF
  - 00
  - 01
  - 02
  - 03

**count is on “1”**

---

### Gates w/ Special I/O Characteristics

- **Schmitt-trigger inputs** (Wakerly, Section 3.7.2, page 130)
  - A special circuit that uses feedback internally to shift the switching threshold depending on whether the input is changing LOW-to-HIGH or HIGH-to-LOW (“hysteresis”)

- **Three-state outputs** (Wakerly, Section 3.7.3, page 132)
  - Output has a third electrical state (not logic state), called high-impedance, Hi-Z, or floating state
  - In this state, the output behaves as if it isn’t even connected to the circuit—the device output “floats” as if it weren’t even there

- **Open-drain (open collector) outputs** (Wakerly, Section 3.7.4, page 133)
  - The output usually comprises an external pull-up resistor, which raises the output voltage when the transistor is turned off
  - Can be rated to withstand a higher voltage than the chip supply voltage
  - Commonly used to drive devices such as Nixie tubes, vacuum fluorescent displays, relays or motors that require higher operating voltages than the usual 5-Volt logic supply
Open-drain (open-collector) outputs

- p-channel transistor provides active pull-up of the output voltage on a LOW-to-HIGH transition
- Omitted in gates with open-drain outputs (see NAND gate below) [called “open-collector” in TTL]
- Example use: driving a light-emitting diode (LED)

![Open-drain CMOS NAND gate](image1)

![Driving an LED with an open-drain output](image2)

Schmitt-Trigger Inverter

It has a hysteresis (difference between the two thresholds) of 0.8 Volts between the low-to-high and high-to-low inputs.

![Schmitt-trigger inverter logic symbol](image3)

![Schmitt-trigger input-output transfer characteristic](image4)
Device Operation w/ Noisy Inputs

noisy, slowly-changing input:

ordinary inverter:

Schmitt-trigger inv.:
(0.8 V hysteresis)

Enabling Function

- **Enabling** permits an input signal to pass through a circuit to an output
- **Disabling** blocks an input signal from passing through to an output, replacing it with a fixed value

The value on the output when it is disable can be Hi-Z (as for three-state buffers and transmission gates, described next), “0”, or “1”

- When disabled, “0” output
- When disabled, “1” output
Three-State Buffers (a.k.a. Drivers)

- For the symbol and truth table, IN is the data input, and EN, the control input.
- For EN = 0, regardless of the value on IN (denoted by X), the output value is Hi-Z.
- For EN = 1, the output value follows the input value.
- Variations:
  - Data input, IN, can be inverted
  - Control input, EN, can be inverted by addition of “bubbles” to signals.

Symbol:

<table>
<thead>
<tr>
<th>EN</th>
<th>IN</th>
<th>OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>Hi-Z</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>Hi-Z</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
</tbody>
</table>

Truth table:

\[ \text{OUT} = \text{IN} \cdot \text{EN} \]

(Logic function, but ignores non-logic connectivity control)

Different Flavors of Three-State

EN_L

OUT_L

EN_L = 1
IN = X
OUT = Hi-Z

74x126 74x125
Three-State Logic Circuit

- Normally, a logic circuit will not operate correctly if the outputs of two or more gates or other logic devices are directly connected to each other (multiple drivers conflict – "fighting")
- Use of three-state logic permits the outputs of two or more gates or other logic devices to be connected together
- Data Selection Function:
  - If \( S = 0 \), \( OL = IN0 \), else \( OL = IN1 \)
- Performing data selection with 3-state buffers:
  \[
  OL = IN0 \cdot S' + IN1 \cdot S
  \]
  - Because \( EN0 = S' \) and \( EN1 = S \), one of the two buffer outputs is always Hi-Z.
  (Recall: when a device output is Hi-Z, it "floats" as if it weren’t even there)

8 Sources Sharing a 3-state Party Line

We can tie multiple outputs together, if at most one at a time is driven.

A decoder circuit … will be described later
Timing Considerations

Timing considerations for the three-state party line

SSRC[20] 7 0 1 2 3
EN1
EN2_L, EN3_L
SDATA

max(\(t_{PLZ_{\text{max}}}\), \(t_{PSZ_{\text{max}}}\)) \quad \text{min}(\(t_{PLZ_{\text{min}}}\), \(t_{PSZ_{\text{min}}}\))

dead time

Three-State Drivers

octal three-state buffer
logic symbol

74x541

G1_L (1)
G2_L (12)

logic diagram

A1 (2) Y1 (19)
A2 (3) Y2 (17)
A3 (4) Y3 (16)
A4 (5) Y4 (15)
A5 (6) Y5 (14)
A6 (7) Y6 (13)
A7 (8) Y7 (12)
A8 (9) Y8 (11)

Note that enable inputs G1_L and G2_L simultaneously enable all eight buffers (i.e., all 8 inputs) — used in bus-based applications, described next …
Buses

- Tristate bus connecting multiple chips:

**Processor**

- from bus
- to bus

**Memory**

- from bus
- to bus

**Video**

- from bus
- to bus

---

Buses - Example

![Diagram of a microprocessor with input ports and user inputs connected to a 74x541 IC and 74138 IC with user inputs and driver application connected to DB0:7]
Three-State Transceivers

Logic diagram

Octal three-state transceiver logic symbol

Enable direction

Direction of transfer

Transceiver Application

Example use of bidirectional transceiver 74x245 to control the direction of data transfer on bidirectional buses