A Low Temperature Coefficient Voltage Reference Utilizing BiCMOS Compensation Technique

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Abstract—This paper presents a low temperature coefficient BiCMOS voltage reference circuit designed in IBM’s SHP Silicon-Germanium (SiGe) technology platform. A BiCMOS compensation approach by combining the temperature properties of HBTs and CMOS transistors has been employed: the Complementary to Absolute Temperature (CTAT) current is generated by a SiGe HBT, while the Proportional to Absolute Temperature (PTAT) current is generated by MOSFETs operating in the subthreshold region. In addition, by adding a nonlinear component, a higher level of temperature compensation is achieved. Simulation results show that with a power supply of 1.2 V, the circuit generates an output voltage of 0.981 V with a temperature coefficient of 0.6 ppm/°C over the temperature range of -25 °C to 125 °C.

I. INTRODUCTION

Silicon-Germanium (SiGe) heterojunction bipolar transistor (HBT) technology utilizes bandgap engineering techniques to develop high performance transistors (with comparable performance to that of III-V transistors), while maintaining compatibility with the conventional low cost Si CMOS manufacturing [1]. The availability of both Si CMOS transistors and high-speed SiGe HBTs, has made the SiGe BiCMOS technology an appealing platform for designing high-speed data converters [2], [3]. One of the main building blocks in data converters that affects their level of accuracy is the high precision reference circuit. It is therefore, essential to develop precise and robust reference circuits in this technology.

Bandgap reference (BGR) circuits are commonly used for implementing stable voltage and current references. In a conventional BGR circuit, a proportional to absolute temperature (PTAT) current/voltage and a complement to absolute temperature (CTAT) current/voltage are added properly, and the circuit generates an output voltage/current that is stable over the desired temperature range. However, due to the existence of non-linear terms in CTAT/PTAT components, a complete temperature compensation is generally not achieved.

Several solutions have been proposed to improve the temperature stability of BGR circuits by employing different curvature compensation techniques to cancel the non-linear terms of the CTAT component [4]-[8]. A popular approach is to apply the Taylor series expansion to the CTAT component, and to design proper compensation circuits to cancel few high-order terms in the Taylor series. In this paper, by combining temperature properties of subthreshold operating CMOS transistors, and the base-emitter junction of SiGe HBTs, we propose a new compensation technique which aims at the complete cancelation of the nonlinear $T \ln(T)$ term in the CTAT component. Advantages of the proposed design include: simplicity, and complete cancelation of the major non-linear term of the CTAT component, resulting in a significant reduction in the variation of the output voltage with temperature.

This paper is organized as follows: in Section II the operation of MOSFETs in the subthreshold regions is described. The proposed technique, circuit architecture, and design methodology are discussed extensively in Section III. Simulation results are presented in Section IV, and conclusions are given in Section V.

II. OPERATION OF MOSFETS IN THE SUBTHRESHOLD REGION

In the subthreshold region, the transistor’s gate-source voltage ($V_{GS}$) is set to be less than its threshold voltage ($V_{TH}$). With drain-source voltage noted as $V_{DS}$, the drain current ($I_D$) for a MOSFET operating in this region is expressed as [9], [10]:

$$I_D = I_S \exp \left( \frac{V_{GS} - V_{TH}}{nV_T} \right) \left[ 1 - \exp \left( -\frac{V_{DS}}{V_T} \right) \right],$$  \hspace{1cm} (1)

where

$$I_S = \frac{W}{L} \mu C_{ox} (n - 1) V_T^2.$$  \hspace{1cm} (2)

In (2), $\mu$ is the carrier mobility, $C_{ox}$ is the gate-oxide capacitance, $V_T$ is the thermal voltage ($V_T = \frac{kT}{q}$, where $k$ is the Boltzmann’s constant), $n$ is the subthreshold slope factor, and $W$ and $L$ correspond to the channel’s width and length, respectively. When $V_{DS} > 3V_T$ (which is generally the case), (1) can be simplified to

$$I_D = I_S \exp \left( \frac{V_{GS} - V_{TH}}{nV_T} \right).$$  \hspace{1cm} (3)

From (3), the expression for $V_{GS}$ can be derived as:

$$V_{GS} = V_{TH} + nV_T \ln \left( \frac{I_D}{I_S} \right).$$  \hspace{1cm} (4)

Replacing (2) in (4), $V_{GS}$ can be re-written as:

$$V_{GS} = V_{TH} + nV_T \ln \left( \frac{W}{L} \mu C_{ox} (n - 1) \right) + 2 \ln(V_T).$$  \hspace{1cm} (5)
Using (6) and (7) in (5), the expression for voltage decreases linearly with temperature as [11]:

\[ V_{TH} = V_{TH0} - \alpha VT(T - T_0), \]  

where \( V_{TH0} \) is the threshold voltage at the reference temperature \( T_0 \), and \( \alpha VT \) is a positive constant. The temperature dependency of the carrier mobility can be estimated as [12]:

\[ \mu = \mu_0 \left( \frac{T}{T_0} \right)^{-m}. \]  

In (7), \( \mu_0 \) is the mobility at \( T_0 \), and \( m \) is a positive constant. Using (6) and (7) in (5), the expression for \( V_{GS} \) of an NMOS transistor operating in the subthreshold region can be written as:

\[ V_{GS} = \gamma_1 + \gamma_2 T + \gamma_3 T \ln(T) + \gamma_4 T \ln(I_D), \]  

where

\[ \gamma_1 = V_{TH0} + \alpha VT_0, \quad \gamma_2 = -\alpha VT - \frac{n k}{q} \ln\left( \frac{W}{C_{ox}} (n - 1)(\mu_0 T_0^m) \right) + 2 \ln(k/q), \quad \gamma_3 = \frac{n k}{q} (m - 2), \quad \gamma_4 = \frac{n k}{q}. \]

### III. PROPOSED VOLTAGE REFERENCE CIRCUIT

The proposed voltage reference circuit consists of four main circuit blocks: the PTAT current generator, the CTAT current generator, a non-linear current generator, and the Vref generator. In this section, details for each circuit block are described.

#### A. PTAT Current Generator

The schematic of the PTAT current generator with its startup circuit is shown in Fig. 1. The startup circuit consisting of transistors \( M_{S1} - M_{S4} \) was also used for starting up the biasing circuit of the operational amplifier [13].

The PTAT generator block employs a floating gate approach using subthreshold MOSFETs, and is a modified version of the structure proposed in [14]. The schematic of the circuit is shown on the right side of Fig. 1. In this circuit, currents \( I_1 \) and \( I_2 \) are designed to be identical. Transistors \( M_3 \) and \( M_4 \) have different aspect ratios and have been biased to operate in the subthreshold region. The difference between the gate-source voltages of these two transistors falls across resistor \( R_1 \), generating current \( I_1 \). From (5), currents \( I_1 \) and \( I_2 \) can be expressed as:

\[ I_1 = I_2 = \frac{V_{GS4} - V_{GS3}}{R_1} = \frac{n V_T \ln \left( \frac{W/L_{14}}{W/L_{24}} \right)}{R_1}. \]  

(9)

As seen from (9), currents \( I_1 \) and \( I_2 \) are proportional to \( V_T \), forming PTAT currents. Since the threshold voltage is a decreasing function of temperature, careful considerations were made in choosing the aspect ratios of transistors \( M_3 \) and \( M_4 \), to ensure they remain operating in the subthreshold operation over the targeted temperature range. Compared to the design in [14], this configuration further improves the performance of the PTAT generator, as it achieves a better mirroring ratio by incorporating a folded-cascode operational amplifier [15] to enforce an identical voltage at the drain terminals of transistors \( M_3 \) and \( M_4 \) (points A and B). Special attention was made to the design of the operational amplifier to make sure it maintains a gain of larger than 60 dB over the desired temperature range (−55 °C to 125 °C). Capacitor \( C_1 \) is driven by the operational amplifier to stabilize the loop. In addition, the current mirrors in [14] were replaced by cascode structures (\( M_{1} - M_{5} \), and \( M_{2} - M_{6} \)).

#### B. CTAT Current Generator

Fig. 2(a) shows the schematic of the CTAT current generator. The CTAT current is generated by utilizing the temperature behavior of the base-emitter voltage \( V_{BE} \) of the SiGe HBT \( (Q_b) \), which, similar to the case of BJTs, is a decreasing function of temperature. The base-emitter voltage of a SiGe HBT can be expressed as [1]

\[ V_{BE} = V_{g0, SiGe} - V_{g0, SiGe} - V_{BE0} T \]

(10)

\[ -\frac{kT}{q} \left\{ \frac{m \ln(T)}{T_0} - \frac{\ln(I_C)}{I_{0, C}} \right\} \]

\[ -\left\{ \frac{kT}{q} \ln \left( 1 - \exp(-\Delta E_{g, Ge(grade)}/kT) \right) \right\} \]

\[ -\left\{ \frac{kT}{q} \ln \left( 1 - \exp(-\Delta E_{g, Ge(grade)}/kT) \right) \right\} \]

where \( V_{g0, SiGe} \) is the extrapolated bandgap voltage of SiGe at 0 K (\( V_{g0, SiGe} = \frac{1}{k} [E_{g0} - E_{g0}^{app} - \Delta E_{g, Ge(grade)}] \)). \( I_{0, C} \), and \( V_{BE0} \) are the reference values of the respective parameters, \( E_{g0} \) is the Si bandgap under low doping, and \( E_{g0}^{app} \) is the bandgap energy in the presence of heavy doping, \( \Delta E_{g, Ge(grade)} \) is the Ge grading-induced bandgap offset, and \( \Delta E_{g, Ge(grade)} \) is the Ge-induced bandgap offset at the emitter end of the neutral base. For the purpose of this design, we will exclude the last two terms of (10), considering that their effects on the overall temperature performance would be negligible. With this assumption, (10) can then be approximated as

\[ V_{BE} \approx \beta_1 + \beta_2 T + \beta_3 T \ln(T) + \beta_4 T \ln(I_C), \]  

(11)

Fig. 1. Schematic of Startup and PTAT current generator circuit.
C. Non-Linear Current Generator

where

\[ \beta_1 = \frac{mK}{q} \ln(T_0) - \frac{V_{g0, SiGe}}{T_0} - \frac{KQ}{q} \ln(I_{C0}), \]

\[ \beta_2 = \frac{mK}{q} \beta_4 = \frac{K}{q} \ln(T_0) - \frac{V_{g0, SiGe}}{T_0} - \frac{KQ}{q} \ln(I_{C0}). \]

As shown in Fig. 2-a, a PTAT current is employed to drive the transistor Q1, while C2 is utilized for compensation in frequency domain. Representing this current with \( \beta T \), where \( \beta \) is a positive constant, (11) can be further simplified to

\[ V_{BE} \approx \beta_1 + (\beta_2 + \beta_4 \ln(\beta_5))T + (\beta_3 + \beta_4)T \ln(T). \] (12)

With the presence of \( T \) and \( T \ln(T) \) terms in \( V_{BE} \) (Equation (12)), it is evident that the CTAT voltage is a complex function of temperature. The goal of the reference circuit is to cancel these temperature dependent parameters and to generate a voltage that is referred to the bandgap energy of the material (in our case \( V_{g0, SiGe} \)). In our proposed circuit, this compensation will be done in the current domain (Fig. 2-b). Therefore, as shown in Fig. 2-a, a current related to \( V_{BE} \) is generated across \( R_3 \).

D. The Vref Generator

Fig. 2-b shows the schematic of the Vref generator circuit. Coefficients \( K_1, K_2 \) and \( K_3 \) are three scaling coefficients which need to be properly determined to generate a reference current that is minimally dependent on temperature. The resulting reference current then flows through resistor \( R_4 \) to generate a temperature stable voltage. We now find the design equations required for determining the coefficients \( K_1, K_2 \) and \( K_3 \). The CTAT current from Fig. 2-a and (12) can be described as

\[ I_{CTAT} = K_1 V_{BE}(Q_1) - \frac{R_3}{K_1 \beta_2 + \beta_3 \ln(\beta_5)}T + (\beta_3 + \beta_4)T \ln(T). \] (13)

Based on (8) and the right hand side of Fig. 3, the nonlinear current can be expressed as

\[ I_{NL} = K_2 \frac{V_{GS}}{R_2} = \frac{K_2}{R_2} \gamma_1 + \gamma_2 T + \gamma_4 T \ln(T) + \frac{\gamma_4 T \ln(I_D)}{R_2}. \] (14)

Next, the PTAT current can be written as

\[ I_{PTAT} = K_3 \gamma_5 T, \] (15)

where \( \gamma_5 = \frac{mK \ln(W/L)}{q}. \) Since in (14), \( I_D \) is a PTAT current \( (\gamma_4 T \ln(I_D)) \), it can be simplified to \( (\gamma_4 \ln \gamma_5) T + \gamma_4 T \ln(T) \). From Fig. 2(b), the output voltage can be written as

\[ V_{REF} = R_4 \left[ \frac{K_1}{R_3} (\beta_2 + \beta_3 \ln(\beta_5)) + \frac{K_2}{R_2} (\gamma_2 + \gamma_4 \ln(\gamma_5)) + K_3 \gamma_5 \right] T \]

\[ + R_4 \left[ \frac{K_1}{R_3} (\beta_3 + \beta_4) + \frac{K_2}{R_2} (\gamma_3 + \gamma_4) \right] T \ln(T). \] (16)

For an optimum design, the coefficients of \( T \) and \( T \ln(T) \) in (16) should be set to zero. Therefore, the following two equations must be satisfied:

\[ R_4 \left[ \frac{K_1}{R_3} (\beta_2 + \beta_3 \ln(\beta_5)) + \frac{K_2}{R_2} (\gamma_2 + \gamma_4 \ln(\gamma_5)) + K_3 \gamma_5 \right] = 0, \] (17)

\[ R_4 \left[ \frac{K_1}{R_3} (\beta_3 + \beta_4) + \frac{K_2}{R_2} (\gamma_3 + \gamma_4) \right] = 0. \] (18)

Since (18) includes the nonlinear term, the design parameters were first set to meet the conditions of (18). After the cancelation of the nonlinear term, the coefficient of \( T \) can be easily adjusted by scaling \( K_3 \) to change the PTAT current and...
to meet conditions of (17). In order to cancel the coefficients of (18), $K_1, K_2, R_2$ and $R_3$ need to satisfy

$$\frac{nK_2}{R_2} = \frac{K_1}{R_1}$$

By placing (19) into (17) we find:

$$k \ln \beta_1 + k \ln \left(\frac{n}{qR_1} \frac{(W/L)_1}{(W/L)_2}\right) + n\frac{k}{q} \ln T_0 + \frac{k}{q} \ln \left(\frac{V_{BE0}}{V_{BE1}}\right) \frac{W}{L} C_{ox} (n-1) T_0 \ln T_0 + \alpha \frac{\gamma}{2} C_{ox} + \ln \left(\frac{q^2}{\gamma^2}\right)$$

It is also important to fine tune $K_3$ to reach the maximum cancellation. When the coefficients of $T$ and $T \ln (T)$ have been compensated, in theory, a temperature independent output voltage equal to $R_4 \left(\frac{K_1}{R_1} \beta_1 + \frac{K_2}{R_2} \gamma_1\right)$ will be achieved.

IV. SIMULATION RESULTS

The proposed reference circuit was designed in IBM’s SiGe 8HP BiCMOS technology and operates with a power supply of 1.2 V. The layout of this circuit is shown in Fig. 4 and occupies an area of 185 $\mu$m x 355 $\mu$m excluding bondpads. Extensive post extraction simulations were performed. The output voltage of the circuit as a function of temperature is shown in Fig. 5. The circuit shows a temperature coefficient of 0.6 ppm/°C across (−25 – 125)°C temperature range and 1.3 ppm/°C across (−55 – 125)°C. Note that since a complete cancelation of temperature coefficients of $V_{BE}$ cannot be done, a non-linear residue appears at the output voltage.

V. CONCLUSION

In this paper, a novel low temperature coefficient current-mode bandgap voltage reference circuit which utilizes a BiCMOS compensation technique was presented. The temperature dependent coefficients of the base-emitter voltage of HBTs are compensated with the PTAT voltage generated by the MOSFETs operating in the subthreshold region. Further temperature stabilization is achieved by incorporating a non-linear current that is also generated by the subthreshold operating NMOS transistors. Based on the simulation results the circuit achieved an excellent temperature coefficient over -25 °C to 125 °C as well as over the military temperature range.

REFERENCES