1) FET INVERTER 5 pts
Prior to T1 the switch has been OPENED. At T1 the switch is CLOSED and is kept closed forever! Plot the following nodes for ~50 us past T1, show all voltage levels, times and time constants. $V_T = 2V$; $K = 1 \text{ mA/V}^2$; $IDS = K(VGS-V_T)^2$.
(a) Plot node 1. 1 pt  
(b) Plot node 2. 1 pt  
(c) Plot $V_o$; show but don't calculate $V_{ol}$ and $V_{oh}$. 1 pt  
(d) Determine the pulse width (time Q is totally cut off), rise time and fall time (10% to 90%) of the output voltage. 2 pt

![FET Circuit Diagram](image)

2) BJT INVERTER 4 pts.
Prior to t0 the switch has been OPEN. At t0 the switch is CLOSED and is kept CLOSED forever. Plot the following nodes for ~10 seconds, show all voltage levels, times and time constants.
$VCE(sat) = 0$, $VBE(on) = 0.7V$, $B = 100$.  
Rs=100Meg, RB1=100Meg, RB2=10K, C=100uF, RC=1K, VCC=10V.
(a) Plot node 1 & node 2. 1 pt  
(b) Plot the current in the capacitor, $I_C$. 1 pt  
(c) Plot $V_o$ showing the pulse width. 1 pt  
(d) Determine the pulse width of the output voltage neglecting the rise and fall times. 1 pt.

![BJT Circuit Diagram](image)
3) BJT INVERTER 4 pts
Prior to t0 the switch has been CLOSED. At t0 the switch is OPENED and is kept opened for 100 u sec. At t1 (100 us after t0) the switch is CLOSED. Plot the following nodes for ~200 us, show all voltage levels, times and time constants.
   a) Plot node 1. 1 pt
   b) Plot node 2. 1 pt
   c) Plot Vo. 1 pt
   d) Determine the width of the generated space (inverted pulse). 1 pt

```
     p 10V
      |
      S

10K

1NF

10K

     p 10V

VCE (SAT) = 0.2V
VBE (ON) = 0.7V

3) JFET with n channel Inverter 7 pts

IDS = 2IDSS/Vp^2 [(VGS-Vp)VDS - VDS^2/2]
IDS = IDSS(1 - VGS/Vp)^2

where Vp = -2 volts and IDSS = 10 mA and Vt is a -5 to +5, 1 KHz square wave.

   a) Plot the voltage at the gate vs time for one cycle starting with VG = -5V. Show voltage levels, times and time constants. 1 pt.
   b) Plot on the same page the output voltage for the same cycle. Show the VOH and VOL voltage levels, rise and fall times. 1 pt.
   c) Determine VOH and VOL 1 pt.
      Assume that VGS − Vp >> VDS and the transistor is ohmic.
   d) Find VGS when Vo is 10 % of VOH. 1 pt
      Find VGS when Vo is 90 % of VOH. 1 pt.
      Assume that the transistor is saturated for both VGS cases.
   e) Find just the rise time of the output voltage. 1 pt.

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```

0 5V

5K

1K

0.05μF

V'(G)

0 5V

5K

1K

0.05μF

```
(5)

\[ V_i(t) \]

\[ V_o(t) \]

\[ B = 100 \]

\[ V_{CE} (sat) = 0.2 V \]

\[ V_{BE} (sat) = 0.7 V \]

Assume \( R_i (\approx 20 k) = 0 \)

\[ V_i(t) \]

\[ 6V \]

\[ 2V \]

\[ 20 \text{ mS} \]

\[ t_0 \]

\[ t_0 + 20 \text{ mS} \]

a) Plot \( V_D \), \( V_B \), \( I_c \), \( I_R \) and \( V_o \)

    considering all circuit elements including \( R_8 \)

b) Compute the time that the output is at 0.2 V

c) Compute the rise time of the output voltage 10\% to 90\%

Due 11 Oct 4:30 PM

Defense 11 Oct 6:30 PM EE 107
6) A normally off inverter shown receives a 0 to 5.7 volt step for an input
Vcc = 10V, Vbb = -4.3V, B = 100, Vce(sat) = 0V, Vbe(sat) = 0.7V.

a) Determine the minimum base current to saturate the transistor. 1 pt.
b) Determine the minimum capacitor current to saturate the transistor. 1 pt.
c) Determine the maximum capacitor current during the step. 1 pt.
d) Determine the time that the transistor remains saturated. 1 pt.
e) Plot the output wave form. 1 pt.
7) BJT INVERTER

Prior to to the switch has been CLOSED. At to the switch is OPENED and is kept opened for 100 u sec. At t1 (100 us after t0) the switch is CLOSED. Plot the following nodes for ~200 us, show all voltage levels, times and time constants.

a) Plot node 1. 1 pt
b) Plot node 2. 1 pt
c) Plot Vo. 1 pt
d) Determine the pulse width of the output voltage. 1 pt

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8) TRANSISTOR INVERTER

For the circuit shown: VCE(sat)=0.2V, VBE(sat)=0.7V, RB=10K, C=1uF
Initially S1 is CLOSED!

a) Plot node B vs time starting when S1 is opened. 1pt
b) Plot V0 vs time starting when S1 is opened (assume that RC is large enough for Q1 to saturate). 1pt
c) Calculate the time from when the switch is opened until when the transistor turns on. 1pt
d) Calculate the minimum value of RC for the transistor to saturate if the transistor beta is 100. 1pt
e) Calculate B(forced) if RC = 1500 ohms. 1pt
MOSFET Inverter with n channel enhancement mode device. Assume that the FET operates in the saturated region for all values of $V_{GS}$ and follows the equation: 

$$I_D = I_{DS} = \frac{1}{2} \left( V_{GS} - V_T \right)^2$$

where $V_T = 4$ volts and $I_{DS} = 1 \text{ mA} \sqrt{\text{V}}$

Initially the switch is closed and at $t=0$ it is opened.

a) Plot the voltage at the gate vs time for 5 sec. 1 pt.
b) Find the time from when the switch is open until the current $I_D$ stops. 1 pt.
c) Find $V_{GS}$ when $V_o$ is 10% of $V_{OH}$.
   Find $V_{GS}$ when $V_o$ is 90% of $V_{OH}$. 1 pt.
d) Find the rise time of the output voltage. 1 pt.
e) Using the information from the above parts plot the output voltage vs time for 5 sec. 1 pt.

![Diagram of MOSFET inverter circuit]

**Note:**

$$I_{DS} = \frac{1}{2} \left( V_{GS} - V_T \right)^2$$

not $I_{DS}$

$$\frac{K}{2} = 1 \text{ mA} / \sqrt{\text{V}}$$
10) FET INVERTER 4 pts
Prior to t₀ the switch has been CLOSED. At t₀ the switch is OPENED and is kept opened for 5 sec. At t₁ (5s after t₀) the switch is CLOSED. Plot the following nodes for 10s, show all voltage levels, times and time constants.

- Assume: \( V_{DS} = 0 \text{V} \) if \( V_{GS} > V_T \) and \( R_D = \infty \) if \( V_{GS} < V_T \) where \( V_T = -2 \text{V} \)
  a) Plot node 1. 1 pt
  b) Plot node 2. 1 pt
  c) Plot \( V_o \). 1 pt
  d) Determine the width of the generated pulse. 1 pt

\[
\begin{align*}
5V & \quad \text{R2 = 1k} \\
1 \mu F & \quad \text{N CHAN} \\
10k & \quad \text{J FET}
\end{align*}
\]

11) MOSFET N channel Inverter 6 pts
\[
\begin{align*}
IDS & = K[(VGS-V_T) VDS - VDS^2/2] \\
IDS & = K(VGS - V_T)^2
\end{align*}
\]
where \( V_T = 1 \text{ volt} \) and \( K = 10 \text{ mA/V}^2 \) and \( V_i \) is a -5 to +5, 1 KHz square wave.

- a) Plot the voltage at the gate vs time for one cycle of the input. Show voltage levels, times and time constants. 1 pt.
- b) Plot on the same page the output voltage for the applied input. Show the VOH and VOL voltage levels, rise and fall times. 1 pt.
- c) Determine VOH and VOL(min). 1 pt.
  For VOH, assume that \( VGS - V_T \) >> VDS & the transistor is ohmic.
- d) Find VGS when Vo is 10% of VOH. 1 pt
  Find VGS when Vo is 90% of VOH. 1 pt.
  Assume that the transistor is saturated for both VGS cases.
- e) Find just the rise time of the output voltage. 1 pt.

\[
\begin{align*}
& \quad \text{R1} \\
& \quad \text{1k} \\
& \quad \text{10V} \\
& \quad \text{V0}
\end{align*}
\]
10) FET INVERTER 4 pts
Prior to to the switch has been CLOSED. At to the switch is
OPENED and is kept opened for 5 sec. At t1 (5s after to) the switch
is CLOSED. Plot the following nodes for 10s, show all voltage
levels, times and time constants.
Assume: \( V_{DS} = 0V \) if \( V_{GS} > V_T \) and \( R_{DS} = \infty \) if \( V_{GS} < V_T \) where \( V_T = -2V \)
   a) Plot node 1. 1 pt
   b) Plot node 2. 1 pt
   c) Plot Vo. 1 pt
   d) Determine the width of the generated pulse. 1 pt

\[ V_O \]
   [Diagram of FET circuit]

11) MOSFET N channel Inverter 6 pts

\[ \begin{align*}
   IDS &= K( (VGS-V_T) VDS - VDS^2/2 ) \\
   IDS &= K( VGS - V_T )^2
\end{align*} \]

where \( V_T = 1 \) volt and \( K = 10 \mbox{ mA/V}^2 \) and \( V_i \) is a -5 to +5, 1 KHz
square wave.

   a) Plot the voltage at the gate vs time for one cycle of the input.
      Show voltage levels, times and time constants. 1 pt.
   b) Plot on the same page the output voltage for the applied input.
      Show the VOH and VOL voltage levels, rise and fall times. 1 pt.
   c) Determine VOH and VOL(min). 1 pt.
      For VOL, assume that \( V_G - V_T >> V_D \) & the transistor is ohmic.
   d) Find VGS when Vo is 10 % of VOH. 1 pt
      Find VGS when Vo is 90 % of VOH. 1 pt.
      Assume that the transistor is saturated for both VGS cases.
   e) Find just the rise time of the output voltage. 1 pt.
(2) EDGE DETECTOR 5 pts
Prior to t1 the switch has been OPEN. At t1=1 sec the switch is CLOSED and is kept closed for 9 sec. At t2 (10 sec after t0) the switch is OPENED. Plot the following nodes for 20 seconds.
N Chan JFET: Vp =-2V; IDSS=10mA; IDS=2IDSS/Vp^2(VGS-Vp) VDS
Show all voltage levels, times and time constants.
a) Plot node 1. 1 pt
b) Plot node 2. 1 pt
c) Determine VCL. 1 pt
d) Plot Vo. 1 pt
e) Determine the pulse width of the output voltage. 1 pt

![Diagram of an edge detector circuit with nodes and voltage levels labeled.]