330:445 Pulse Circuit Homework and Solutions

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1) RC Filter Ckt 3 pts.

Input voltage, $V_i$, is a 0V to +10V pulse train with 30% duty cycle and a freq of 1 KHz.

a) Sketch the output wave form showing $V_{oH(SS)}$, $V_{oL(SS)}$, PW, and Ts.
b) Determine $V_{oH(S)}$ and $V_{oL(SS)}$.

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2) CLAMP CIRCUIT 3 pts.

A 0V to -10V, 500 Hz square wave is applied to the clamp circuit shown:

$C=10\mu F$, $R=2\Omega$, $V_{bias}=-5V$, $V_F=0.7V$

a) Determine the steady state capacitor voltage. 1 pt

b) Sketch 2 cycles of the output wave form for the applied input showing: all voltage levels, times and tilt. 1 pt.

c) Calculate the tilt. 1 pt.
3) CLAMP CIRCUIT  5 pts.
A +5V and -5V  500 Hz square wave is applied to the clamp circuit shown: C=100uF, R=1K, Vz=3V

a) Determine the output clamp voltage Vo(C).  1 pt.
b) Determine the steady state capacitor voltage. 1 pt

c) Determine the voltage across the resistor when the diode is Reversed biased 1 pt.

d) Calculate the tilt in the output waveform 1 pt.

e) Sketch 2 cycles of the output waveform for the applied input showing: all voltage levels, times and tilt. 1 pt.

\[ V_F = 0.7V \]
OP-AMP 4 pts.

For the following circuit:
a) Plot node 1 vs. time for the applied input voltage. 1 pt
b) On one page plot Vo vs. time, below Vi vs. time, for at least one cycle. Show voltage levels. 2 pt
c) Determine the value of R3 to DC null the output. 1 pt

R1=10K; R2=100K; VF(D1)=0.7V; VBB=5V
Initially $S_1$ is CLOSED and circuit reaches steady state ($I_C=0$). At $t(0^+)$ $S_1$ is OPENED and is kept OPENED until circuit reaches steady state ($I_C=0$). Then is $S_1$ CLOSED again and is kept CLOSED until circuit reaches a steady state condition.

For the following plots show all voltage (current) levels, times, and time constants.

a) Plot the node voltage at node 1. 1 pt.
b) Plot the node voltage at node 2. 1 pt.
c) Plot the capacitor current. 2 pts.
d) Calculate the time it takes from when the switch is closed again till the diode $D_2$ turns on. 1 pt.
6) A negative square wave is applied to the clamp circuit shown:

a) Determine the output clamp voltage $V_o(C)$. 1 pt.
b) Determine the steady state capacitor voltage and indicate polarity 1 pt.
c) Determine the voltage across the resistor when the diode is Reversed biased 1 pt.
d) Calculate the tilt in the output waveform 1 pt.
e) Sketch 2 cycles of the output waveform for the applied input showing: all voltage levels, times and tilt. 1 pt.

\[ V_F = 0.7 \]

\[ C \]

\[ \frac{50 \mu F}{R \quad 1K \quad V_o(t)} \]

\[ V_i(t) \quad f = 500 Hz \]
7) Diode Clamping Ckt with Zener

f = 500 Hz

R1=5K; C1=1uF; VF(D1,D2)=0.7V; VB(D2)=5V

a) Plot Vo, label voltage levels and times. 5 pts.
b) Find VC at steady state. 5 pts.
c) Find IR1 when Vi = -10V. 5 pts.
d) Find ΔVo when Vi = -10V. 5 pts.
e) Find the Tilt and show tilt on part (a) plot 5 pts.
$\text{RC CIRCUIT}$

For the circuit and the applied input shown:

a) Write an expression for the output voltage in terms of the input voltage and the circuit time constant. 2 pts

b) Plot the output voltage vs time for 10 usec. showing all voltage levels and times. 2 pts
Capacitor Coupled Circuits (edge detectors): Initially S1 is opened and circuit reaches steady state (Ic=0). At t(0+) S1 is closed and is kept closed until circuit reaches steady state (Ic=0). Then is S1 opened again and is kept opened until circuit reaches a steady state condition.

Plot for each of the following circuits: Ic and nodes 1 and 2 during the above switch operations. (Show all voltage (current) levels, times, time constants, initial conditions and recovery.)
A ± 10V square wave is applied to a zener diode SHUNT clipper circuit which will clip off input peaks greater than 6 volts.

Maximum output current = 2 mA
Allow 5 mA of zener current to establish zener voltage

a) Sketch the circuit (indicate proper direction for diodes) 2 pts.
b) Determine R 1 pt.
c) Sketch the output wave form 1 pt.
d) Compute the power in each diode. 1 pt.