Homework #5: TTL

Question #1: TTL inverter

$B_R = 0.1, B_F = 30, V_{BE(OFF)} < 0.5V, V_{BE(ON)} = 0.7V, V_{CE(sat)} = 0.2V, \tau_S = 10\, ns, R_1 = 1k\Omega. VCC = 5V.$

\[\text{a. Find } V_{IL}\]
\[\text{b. Find } I_{IL} @ V_i = V_{IL}\]
\[\text{c. Find } V_{IH}\]
\[\text{d. Find } I_{IH} @ V_i = V_{IH}\]
\[\text{e. } I_{B2F} @ V_i = V_{IH}\]
\[\text{f. } I_{B2r}, \text{ when } V_i \text{ goes from } V_{IH} \text{ to } V_{IL}\]
\[\text{g. } I_{B2(EOS)} @ V_i = V_{IH}\]
\[\text{h. Find } T_S, \text{ the storage time.}\]

Question #2: TTL Nand Gate

$V_{BE(Sat)} = 0.7V, V_{CE(Sat)} = 0.2V, B_F = 20, B_R = 0.2, V_{D1(on)} = V_{D2(on)} = 0.3V, V_{D3(on)} = 0.7V$ (questions on the next page)
a. Find $I_{IL}$ if $V_i = 0.2V$ and both inputs are low.
b. Find $I_{IH}$ if $V_i = 3V$ and both inputs are high.
c. Find $I_{o(\text{Max})}$ @ $V_i = 3V$.
d. Find $I_{o(\text{Max})}$ @ $V_i = 0.2V$ and $V_o = 3V$.
e. Find Fan Out Low with worst case input condition.
f. Find Fan Out High for $V_o = 3V$.

Question #3: TTL Gate

$B = 50$, $B_R = 0$, $V_{CE\text{(sat)}} = 0.2V$, $V_{BE\text{(on)}} = 0.7V$, $V_{BE\text{(Off)}} < 0.5V$, $V_{D\text{(on)}} = 0.7V$, $V_{D\text{(off)}} = < 0.7V$

a. Find $V_{IL}$.
b. Find $I_{IL}$, if $V_{i1} = 0.1V$ and $V_{i2} = 0.1V$.
c. Find $I_{IL}$, if $V_{i1} = 0.1V$ and $V_{i2} = 5V$.
d. Find $V_{IH}$ (Minimum).
e. Find $I_{o(\text{MAX})}$ if $V_{i1} = V_{i2} = 5V$ (Do not neglect $R_{B3}$ and $R_{C3}$).
f. Find $I_{o(\text{MAX})}$ if $V_{i1} = 0.1V$, $V_{i2} = 5V$ (Do not neglect $R_{B3}$ and $R_{C3}$).
g. Find Fan Out Low with conditions of part b. and part f.
Question #4: DTL gate. $V_{BE\text{(cut-in)}} = 0.5\text{V}$, $V_{BE\text{(Sat)}} = 0.7\text{V}$, $V_{CE\text{(Sat)}} = 0$, $B = 20$, $V_{D\text{(on)}} = 0.7\text{V}$.

a. Find $V_{iL}$.
b. Find $V_{iH}$ for $I_o = 0$, and one input high.
c. Repeat part B for both inputs high and $I_o = 10\text{mA}$.
d. What is the Fan Out for the output low state?
e. What is the Fan Out for the output High State driving similar gates with the input conditions ($V_{IH}$) of part B.

Question #5: TTL Gate

$V_{CE\text{(sat)}} = 0.2\text{V}$, $V_{D\text{(ON)}} = V_{BE\text{(On)}} = 0.7\text{V}$, $V_{BE\text{(off)}} < 0.5\text{V}$, $B_{L\text{(Lateral)}} = 1$, $B_R = 0.5\text{V}$, $B_F = 20$.

a. Find $V_{iL}$ (maximum).
b. Find the worst case $I_{iL}$ when $V_i = 0.3\text{V}$. (More on the next page)
c. Find $V_o$ when $V_{i1} = V_{i2} = 0\text{V}$ and $I_o = +5\text{mA}$

d. Find the Maximum $I_o$ if $V_{i1} = 3\text{V}$ and $V_{i2}$ is open circuited.

e. What would the fan out to be for the conditions of part B combined with part D.

**Question #6: TTL Gate**
The output of the TTL gate shown is accidentally shorted to ground. Determine the short circuit current when:

$B = 20, V_{D(on)} = 0.7\text{V}, V_{CE(Sat)} = 0.2\text{V}, V_{BE(on)} = 0.7\text{V}$

- All inputs are at a logic "1"
- At least one input is at a logic "0"

**Question #7: Fan Out** (questions on the next page)

The inverter shown has the following parameters: $B_F = 25, B_R = 0.5, V_{CE(sat)} = 0.3\text{V}, V_{D(on)} = 0.7\text{V}, V_{BE(sat)} = 0.7\text{V}, V_{BE(off)} < 0.7\text{V}$. (Note the unusual value for $V_{BE(off)}$.)
a. Determine the maximum $V_i$ and the associated $I_i$ for a $V_o = 5V$ where $Q2$ is off.
b. Determine $I_{E1}$ and $I_{B2}$ for $V_i = 3$ to 5 Volts.
c. Determine the logic "0" fan out to $N$ identical gates where $V_i = 5V$ and $V_o$ equals the voltage value calculated for $V_i$ in part A.
d. Determine the logic "1" fan out to $N$ identical gates when $V_i = 0$ and $V_o = 3V$.

Question #8: DTL Gate
$V_{BE(on)} = 0.7V$, $V_{BE(off)} < 0.5V$, $V_{CE(sat)} = 0.2V$, $B = 10$, $V_{D(On)} = 0.2V$

a. Find $V_{iL}$.
b. Find $I_{iL}$ worst case @ $V_i = 0V$ (Hint: $Q1 = sat$)
c. Find $V_{iH}$
d. Find $I_{iH}$ at $V_i = 5V$
e. Find $I_{B2}$ when $V_{i1} = V_{i2} = 5V$
f. Find $I_{B2r}$ the instant that $V_i$ goes for $V_{iH}$ to $V_{iL}$. Include the effects of $R_{B2}$ and $Q1$.

Question #9: TTL Gate. Circuit drawing on the next page.
$V_{CE(sat)} = 0.2V$, $V_{D(ON)} = V_{BE(on)} = 0.7V$, $V_{BE(off)} < 0.5V$, $B_L$ (lateral) = 1, $B_N = 20$, $B_R = 0.5$.

a. Find $V_{iL}$
b. Find $V_{iH}$
c. Determine the states of each of the four transistors when all inputs are at a logic one.
d. Find $I_o$ when the output is shorted to ground and the conditions of Part C are applied.
e. Determine the states of each of the four transistors when at least one of the inputs are at a logic zero.
f. Find $I_o$ when the output is shorted to ground and the conditions of part E are applied.
Circuit drawing is on the next page.

Solutions will also be posted to questions: 12, 13, 15, 17, 18 and 19 from Chapter 14 in Sedra and Smith.