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Design of 1.7 to 14kV Normally-Off Trenched and Implanted Vertical JFET in 4H-SiC

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Abstract. In this paper, a high voltage normally-off trenched-and-implanted vertical JFET (TI-VJFET) in 4H-SiC is investigated by way of two-dimensional numerical simulations. The structure is simple to fabricate and is expected to be able to achieve a high current density. Detailed designs are presented for 1.7kV to 14kV normally-off 4H-SiC VJFETs. A good agreement has been reached between computer modeling and experimental 1.7kV normally-off TI-VJFET in 4H-SiC. The fabricated 1.7kV device shows a $V_B^2/R_{on,sp}$ value of 827MW/cm^2 at room temperature, which represents a substantial performance improvement to the state-of-the-art.

Introduction

In recent years, a large effort has been devoted to the development of SiC power switches because they are expected to drastically outperform their Si counterparts for high power and high temperature applications. Among the unipolar power switching devices, SiC MOSFET and JFET have recently been investigated intensively. SiC JFET is advantageous over SiC MOSFET in that SiC MOSFET currently suffers from low channel mobility [1] and may have reliability problems when operated under both high electric fields and high temperatures [2]. This paper presents the design of a high-voltage normally-off trenched-and-implanted vertical JFET (TI-VJFET) in 4H-SiC. In comparison to previously reported VJFETs [3,4], this device is simpler to fabricate because it (i) does not need the expensive epitaxial re-growth, (ii) eliminates the lateral JFET, making it possible to achieve near theoretical performance over a wide voltage range, and (iii) only one mask requires critical alignment. It is shown that this structure can be readily used to fabricate TI-VJFETs with different blocking capabilities in a single fabrication run by simply using the appropriate thickness and doping concentration for the drift layer. The TI-VJFET structure is optimized using ISE-TCAD device simulator with the physical models of 4H-SiC as depicted in [5]. A good agreement has been reached between theoretical and experimental 1.7kV normally-off 4H-SiC TI-VJFET.

Device Structure of 14kV TI-VJFET

The cross sectional view of the 14kV TI-VJFET is shown in Fig.1. This structure has been optimized to block over 14kV in normally-off mode by performing a lot of trial simulations. It consists of three N-type epilayers. The top heavily doped N^+ epilayer is used for the source ohmic contact. The middle N-type epilayer, which has a thickness of 2.6μm and a doping concentration of 5×10^{15}cm^{-3}, is used to form the vertical channel. The vertical channel is designed to be completely depleted at zero gate bias at both room temperature (RT) and 200°C so that the device can operate in normally-off mode up to 200°C. The bottom

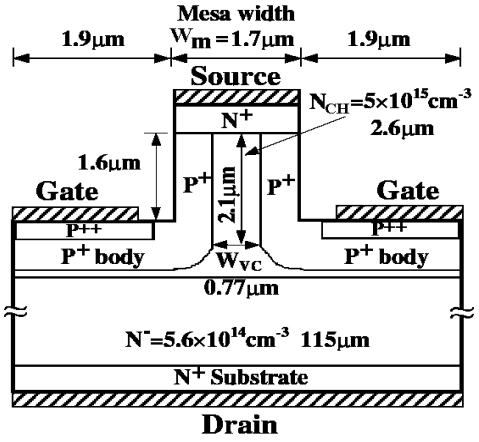


Fig.1. 14kV TI-VJFET cell structure.

lightly doped N^- layer, which has a thickness of 115μm and a doping concentration of $5.6\times10^{14}cm^{-3}$, is used to support high drain voltage. The deep gate trench is to be created by using ICP etching. Multi-step Al-implantation can be applied to form the vertical channel and P^+ trench bottom for gate ohmic contact.

DC Characterization of 14kV TI-VJFETs

Gate Voltage. To turn on the device, a positive voltage must be applied on the gate to forward bias the junction between the gate P^+ region and the N-type channel layer. The maximum gate voltage that can be used to turn on the device is limited by the allowed maximum gate current density, which is set to be $1A/cm^2$ in this work. Therefore, the maximum gate voltage used to turn on the device is 2.75V and 2.45V at RT and 200ºC, respectively, as depicted in Fig.2.

Forward and Blocking Characteristics. The forward and blocking characteristics of the optimized device are presented in Fig.3. At RT, the forward current density is $33.9A/cm^2$ at V_D equal to 5V, corresponding to a specific on-resistance of $147.5m\Omega\cdot cm^2$, which is close to the specific on-resistance ($139.5m\Omega\cdot cm^2$) of the drift layer. Obviously, the drift layer resistance dominates the device total on-resistance. At 200ºC, the forward current density is $14.24A/cm^2$ at V_D equal to 5V, corresponding to a specific on-resistance of $351m\Omega\cdot cm^2$. It is seen from Fig.3b that the device can block 14,316V and 14,976V in normally-off mode at RT and 200ºC, respectively.

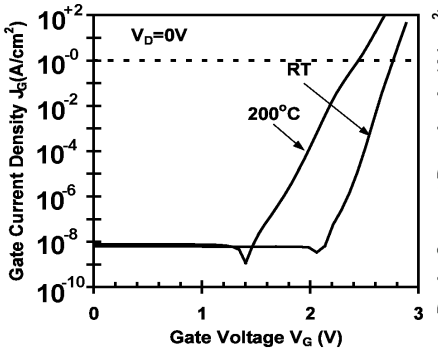


Fig.2. Dependence of gate current density on gate voltage.

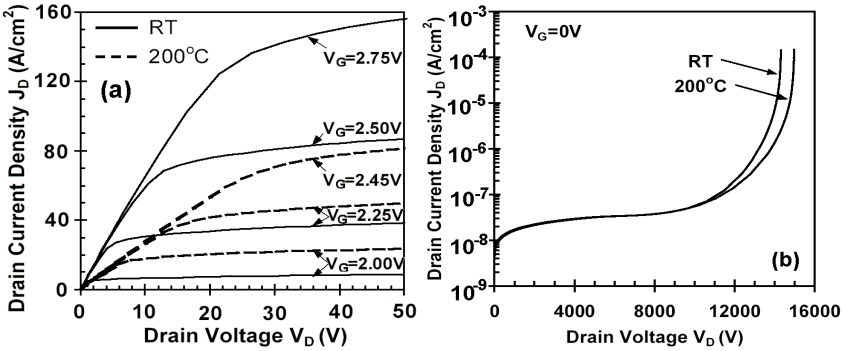


Fig.3. Forward (a) and blocking (b) characteristics of normally-off 14kV TI-VJFET.

Design of Mesa Width (W_m) and Vertical Channel Doping Concentration (N_{CH})

For a normally-off device, the leakage current density in off-state should be as low as possible. In this design, the maximum allowed leakage current density is set to be $1mA/cm^2$. The effects of W_m and N_{CH} on the device blocking characteristics at RT are shown in Fig.4. The vertical channel opening W_{VC} at $N=5\times10^{15}cm^{-3}$ is 0.77μm and 1.02μm for W_m equal to 1.7μm and 1.95μm, respectively. It is seen from Fig.4 that, to keep the leakage current density lower than $1mA/cm^2$ at 14kV, the maximum N_{CH} must be lower than 9×10^{15} cm^{-3} and 3×10^{15} cm^{-3} for W_m equal to 1.7μm and 1.95μm, respectively. It also can be seen from Fig.4 that N_{CH} has almost no effect on the avalanche breakdown voltage. This makes it possible to design the channel layer and blocking layer separately for high voltage normally-off TI-VJFETs.

To optimize W_m (or W_{VC}) and N_{CH}, their effects on the device forward characteristics are simulated and presented in Fig.5. For W_m = 1.7μm (W_{VC} = 0.77μm at $N=5\times10^{15}cm^{-3}$), the drain current density does not saturate for V_D up to 40V when N_{CH} is larger than $7\times10^{15}cm^{-3}$. But, for W_m = 1.95μm (W_{VC} = 1.02μm at $N=5\times10^{15}cm^{-3}$), the drain current density saturates at a relatively low current density of $130A/cm^2$ even when the maximum allowed N_{CH} of $3\times10^{15}cm^{-3}$ is used.

Therefore, W_m should not be too wide. A W_m of 1.7μm is a good choice. W_m, however, can not be too small because it is difficult to process.

Because the device is designed to operate up to 200°C, the effects of W_m and N_{CH} on the device characteristics at 200°C for W_m = 1.7μm are simulated and shown in Fig.6. It is seen that the leakage current density at 14kV is slightly larger than 1mA/cm^2 when $N_{CH} = 7\times10^{15}$cm^{-3}. Thus, the maximum allowed N_{CH} is about 7×10^{15}cm^{-3} in order to keep the device normally off at both RT and 200ºC. Considering the fact that the doping concentration in commercial wafer could be 50% off the expected value, a N_{CH} of 5×10^{15}cm^{-3} is used in the optimized 14kV TI-VJFET.

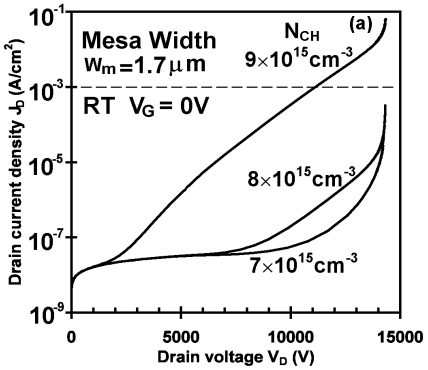


Fig.4. Effects of mesa width and channel doping concentration on the blocking characteristics of 14kV TI-VJFET at RT.

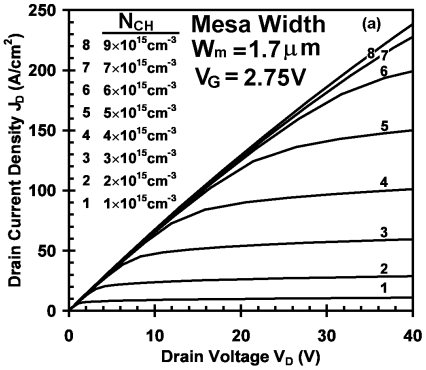


Fig.5. Effects of mesa width and channel doping concentration on the forward characteristics of 14kV TI-VJFET at RT.

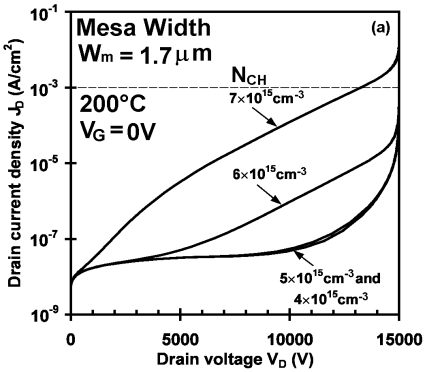
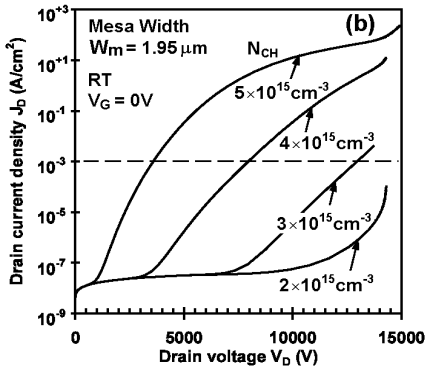
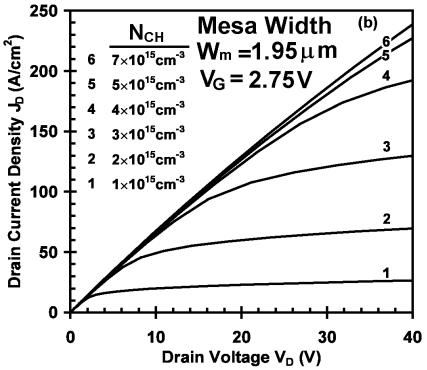
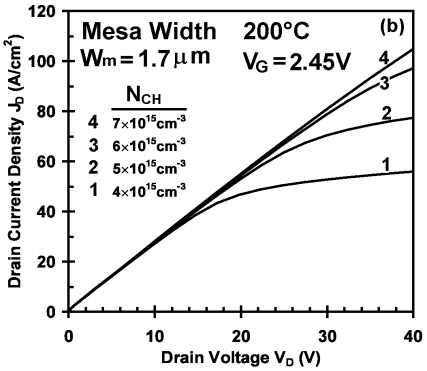


Fig.6. Effects of channel doping concentration on the blocking characteristics of 14kV TI-VJFET at 200°C.







Drift Layer Design for 1.7 to 14kV TI-VJFETs

Different blocking capabilities can be realized for the TI-VJFET shown in Fig.1 by simply using the proper thickness W_D and doping concentration N^- for the drift layer without changing the gate and source design. For punch through structure, W_D and N^- can be optimized to give the lowest specific on-resistance. The optimized W_D and N^- for different voltage normally-off TI-VJFETs and the corresponding specific on-resistance of the TI-VJFETs at RT and 200ºC are shown in Fig.7. When the blocking voltage is lower than 3kV, it is seen from Fig.7 that N^- is close to or even larger than the optimized $N_{CH} = 5\times10^{15}$cm^{-3}. Thus, the same doping concentration is used in the channel layer and the blocking layer in Fig.7 when the blocking voltage is lower than 3kV.

Comparison between Modeling and Experimental Results

A 1.7kV normally-off 4H-SiC TI-VJFET has been demonstrated experimentally. Detailed fabrication steps can be found in [6]. The measured DC characteristics are presented in Fig.8. A near theoretical blocking voltage (V_{bl}) of 1,726V has been achieved with a low specific on-resistance of

3.6mΩ-cm^2, giving a $V_{bl}^2/R_{on,sp}$ value of 827MW/cm^2, which represents a substantial performance improvement to the state-of-the-art. Simulations have been performed to evaluate the vertical channel mobility, as shown in Fig.8. A good agreement between the experimental and modeling results is obtained when the channel electron mobility is 561cm^2/Vs, W_{VC} is 0.63μm, and N_{CH} is 6.5×10^{15}cm^{-3}, which are very close to the designed values.

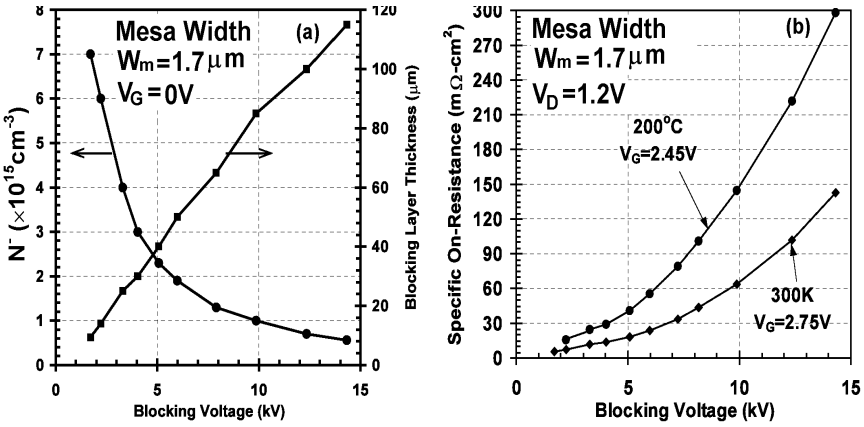


Fig.7. Optimized drift layer for 1.7 to 14kV TI-VJFETs (a) and corresponding device specific on-resistance.

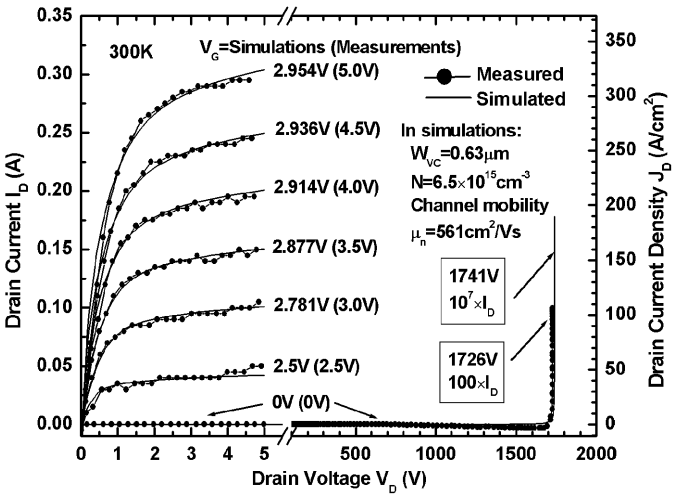


Fig.8. Measured and simulated DC characteristics of a fabricated 1.7kV normally-off TI-VJFET in 4H-SiC at RT.

Summary

1.7kV to 14kV 4H-SiC normally-off TI-VJFETs have been designed and optimized by performing a large number of numerical simulations. A good agreement between theoretical and experimental results has been achieved for a 1.7kV TI-VJFET and channel electron mobility, opening and doping concentration have been evaluated.

Acknowledgement

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References

[1] J. A. Cooper, Jr., M. R. Melloch, R. Singh, A. Agarwal, and J. W. Palmour: IEEE Trans. Electron Devices, Vol. 49 (2002), p.665.

[2] M. M. Maranowski and J. A. Cooper, Jr.: IEEE Trans. Electron Devices, Vol. 46 (1999), p.520.

[3] P. Friedrichs, H. Mitlehner, R. Schörner, K.-O. Dohnke, R. Elpelt, and D. Stephani, Materials Science Forum, 2002, vols. 389-393, p. 1185-1188.

[4] K. Asano, Y. Sugawara, S. Ryu, R. Singh, J. Palmour, T. Hayashi, and D. Takayama, ISPSD 2001, p.23-26

[5] J. H. Zhao, X. Li, K. Tone, P. Alexandrov, M. Pan and M. Weiner: Solid-State Electronics, Vol. 47 (2003), p.377-384

[6] J. H. Zhao, K. Tone, X. Li, P. Alexandrov, L. Fursin and M. Weiner : ISPSD 2003, Cambridge, UK, p.50-53.