High Power (500V-70A) and High Gain (44-47) 4H-SiC Bipolar Junction Transistors

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Abstract. This paper reports high power 4H-SiC BJTs with record high current handling capabilities. Wet-oxygen low-temperature re-oxidation and aluminum-free Ohmic contacts were applied in the fabrication processing. Up to 7A (Ic=583A/cm²) with a single BJT cell has been achieved at VCE=5.5V. The peak DC common emitter current gain reached 47 at Ic=4.7A (Jc=392A/cm²) and Vce=6.5V. The open base blocking voltage (Vceo) reached up to 858V with 1mA leakage current. The specific on-resistance was measured to be 8.7mΩ⋅cm² up to Ic=5.5A (Jc=458A/cm²) at Vce=4.0V. At 150°C, the peak current gain was still as high as 36 at Ic=3.6A at Vce=10V. The specific on-resistance at 150°C was 13.2mΩ⋅cm² up to Ic=4.0A (Jc=333A/cm²) at Vce=4.4V. At 100°C, the open base blocking voltage was measured up to 875V with 1mA leakage current. A 4H-SiC BJT package containing nine similar BJT cells was also fabricated and tested. The highest collector current was measured up to 70A. The peak DC current gain was 44.3 at Ic=44.3A (Jc=410A/cm²) and Vce=5.5V. The open base blocking voltage for the package at 500V showed a leakage current of 8mA. Its inductively-loaded half-bridge switching results are also reported.

Introduction

4H-SiC is a promising material for high power and high temperature applications. 4H-SiC BJTs are free of gate oxide problems and can provide high current with low forward voltage drop. The first high power 4H-SiC BJTs were presented in a conference in June 2000[1,2] and published in a journal in August 2000[3]. Subsequently, high voltage 4H-SiC BJTs were reported, including (i) a 1800V 4H-SiC BJT with a maximum β=20, Ic,MAX= 3.8A (Jc=271A/cm²) at VCE=5V and a specific on-resistance (RSP_ON) of 10.8 mΩ⋅cm² at Jc=193A/cm² by using a drift layer of 20µm doped to 2.5x10¹⁵ cm⁻³ [4]; (ii) a 4H-SiC BJT with Vceo >3200V and a β = 15 at Ic = 1.2A (Jc=115A/cm²) by using a drift layer of 50µm doped to 8x10¹⁴ cm⁻³ [5]; (iii) a 500V 4H-SiC BJT based on a 20µm, 2.4x10¹⁵ cm⁻³ doped drift layer, showing current gains over 50 and an RSP_ON of 26mΩ⋅cm² [6,7]; and (iv) a 480V 4H-SiC BJT with a β =38 at Jc=114A/cm² and an RSP_ON of 14 mΩ⋅cm² based on a 12µm, 6x10¹⁵ cm⁻³ doped drift layer [8]. Because BJT current gain can be increased by reducing the base doping concentration or thickness which leads to lower blocking performance, it is important to demonstrate BJTs capable of simultaneously high current gain and high blocking voltage. This paper reports 4H-SiC BJTs capable of 850V-7A by single cell with a peak DC current gain of 47 and an RSP_ON=8.7mΩ⋅cm² up to Jc=458A/cm², and a high current packaged BJT of 500V-70A based on nine high performance BJT cells.

Device Design and Fabrication

A cross-sectional view of the 4H-SiC BJT structure is shown in Fig.1. Three epi-layers were grown on the 8° off-axis n-type 4H-SiC substrate. The top n⁺ epi-layer of 0.7µm was heavily doped to
$2 \times 10^{19} \text{cm}^{-5}$ to serve as the emitter. The base p-type layer of 0.8μm was doped to $3 \times 10^{17} \text{cm}^{-3}$. The collector drift layer of 12μm was lightly-doped to $6 \times 10^{15} \text{cm}^{-3}$.

The emitter mesa was defined by inductively coupled plasma (ICP) etching in a gas mixture of freon and oxygen at an etching rate of 70-80nm/min. The emitter mesa etching depth was 0.82μm. The base implantation was done at room temperature with multiple carbon and aluminum co-implantation, which consists of C ions of $4 \times 10^{14} \text{cm}^{-2}$ at 28keV, $5.2 \times 10^{14} \text{cm}^{-2}$ at 60 keV, and $1.1 \times 10^{14} \text{cm}^{-2}$ at 75 keV plus Al ions of $3.6 \times 10^{14} \text{cm}^{-2}$ at 50 keV and $7.5 \times 10^{14} \text{cm}^{-2}$ at 100 keV. The designed spacing between the implanted base region and the emitter mesa edge was 5μm, because too small a spacing between the implanted base region and the emitter edge has been shown to reduce transistor current gains\[5\]. Post-implantation annealing was done at 1550°C for 30 min in Ar. A single step JTE of 160μm wide based on the existing p-type base epilayer was used for the edge termination. The isolation between each device was served by a mesa etching of ~1.4μm into the drift layer. As wet-oxygen low-temperature re-oxidation has been shown to reduce SiO$_2$/SiC interface defect density [9], the samples were re-annealed in wet-oxygen for 2 hours at 950°C after a regular wet thermal oxidation for 2 hours at 1100°C followed by a one-hour Ar annealing at 1100°C. After the thermal oxidation, 250nm SiO$_2$ and 250nm Si$_3$N$_4$ were deposited by PECVD to seal the thermal passivation layer.

Because previous results [8,10] showed that Al-free base contact could eliminate the possible Al-spiking during the Ohmic contact annealing, 200nm Ti covered by 200nm TiN were sputtered as the Ohmic contact metal for both base and emitter. The collector contact metal was 20nm AlTi covered by 700nm Ni on the substrate. The Ohmic contact annealing was carried out for 8 minutes at 1050°C in nitrogen forming gas (5% H$_2$ in N$_2$). The emitter n-type specific contact resistance and $n^+$ emitter layer sheet resistance were $8.6 \times 10^{-6} \Omega \cdot \text{cm}^2$ and 236Ω respectively, while the p-type specific contact resistance and p-base sheet resistance were $0.6 \Omega \cdot \text{cm}^2$ and 58 kΩ, respectively. After Ohmic contact formation, layers of 414nm SiO$_2$ and 250nm Si$_3$N$_4$ were deposited by PECVD for the insulation between the overlay metals. The base and emitter contact windows were opened by ICP, and the overlay metals of Ti(50nm) and Au(1.54μm) were deposited and patterned to form the base and emitter bonding pads. The collector overlay metal was 100nm Ni and 700nm Au on the substrate.

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Fig.2 shows a microscopic photo of a fabricated BJT device. Excluding the bonding pads and the edge termination region, the device active area is 1.2mm$^2$. The total device dimension is 1.57mm×1.66mm. Each device contains 37 emitter fingers with the dimension of 1186μm×14μm.
Characterization and Discussion

Fig. 3 shows the I-V characteristics of a BJT cell at room temperature. The peak DC current gain is 47 at $I_c=4.7A$ ($J_c=392A/cm^2$) and $V_{ce}=6.5V$ at room temperature. The maximum collector current was measured up to 7.1A ($J_c=592A/cm^2$). The specific on resistance was 8.7$m\Omega\cdot cm^2$ up to $I_c=5.5A$ ($J_c=458A/cm^2$) at $V_{ce}=4.0V$. The open base blocking voltage ($V_{ceo}$) was measured up to 858V with 1mA leakage current. Fig. 4 shows the I-V characteristics measured at 150$^\circ$C. The peak DC current gain was still as high as 36 at $I_c=3.6A$ ($J_c=300A/cm^2$) and $V_{ce}=10V$. The specific on resistance increased to 13.2$m\Omega\cdot cm^2$ at $I_c=4.0A$ ($J_c=333A/cm^2$) and $V_{ce}=4.4V$. The open base blocking was measured up 875V at 1mA leakage current at 100$^\circ$C.

Fig. 3. BJT I-V characteristics at RT.

Fig. 4. I-V characteristics at high temperatures.

Fig. 5 shows the DC current gain versus the collector current density at $V_{ce}=10V$. This single cell BJT capable of 850V-7.1A, 8.7$m\Omega\cdot cm^2$ (at $J_c=458A/cm^2$) and a $\beta=47$ is among the best of the high gain 4H-SiC BJTs reported to date[7].

Nine BJT cells in the same chip with similar I-V characteristics were die-mounted in a power package and ribbon-bonded to form a high current BJT package. Fig. 6 shows the I-V curves of the 4H-SiC BJT package. The current was measured up to 70A. The peak DC current gain for this whole package was 44.3 at $I_c=44.3A$ ($J_c=410A/cm^2$) and $V_{ce}=5.5V$. The specific on-resistance was 10$m\Omega\cdot cm^2$ up to $I_c=56.9A$ ($J_c=527A/cm^2$) at $V_{ce}=5.35V$. The open-base blocking voltage of the whole package was measured up to 500V with a leakage current of 8mA. This 500V-70A 4H-SiC BJT package with a high DC current gain 44.3 is the best performing SiC BJT demonstrated to date considering both the high current and high gain achieved.

Comparing to the previous BJTs[3,8,10], some processing modifications were believed to be the reason for this high gain, high performance 4H-SiC BJT. The low-temperature wet-oxygen re-oxidation could reduce SiO$_2$/SiC interface defect density, which leads to a better passivation on both the base-emitter junction and the base-collector junction. The Al-free base contact metal (Ti/TiN) eliminated the possible Al-spiking problem as reported before[7], hence resulted in a better device blocking performance.
The 4H-SiC BJT package was also tested in an inductively-loaded half-bridge inverter with SiC MPS(Merged-PiN-Schottky) diode serving as the freewheeling diode. The inductive load was 1mH to simulate a high power induction motor. The switching experiment was carried out at a bus voltage of 320V and a switching current of 30A. Results showed that the collector current (Ic) has a turn-on rise time of 0.10µs and a turn-off fall time of 0.14µs. The turn-on switching energy loss was 1.33mJ, while the turn-off energy loss was 0.77mJ.

Summary

A high gain, high power 4H-SiC BJT capable of at least 850V-7.1A has been demonstrated in 4H-SiC using a drift layer of 12µm doped to 6x10^{15} cm^{-3}. The BJT achieves a DC current gain around 47 at J_C = 392A/cm^2 and an R_SP_ON of 8.7 mΩ·cm^2 up to a high Jc of 458 A/cm^2. A nine-cell high current gain (β=44.3) 4H-SiC BJT package capable of at least 500V-70A has also been demonstrated. Its inductively loaded half-bridge switching measurement resulted in a turn-off time of 0.14µs and a turn-off switching energy loss of 0.77mJ.

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