A Novel, Planar 3,000 V Normally-Off Field Gated Bipolar Transistor in 4H-SiC

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Abstract. In this paper, a novel planar high-voltage normally-off 4H-SiC field gate bipolar transistor (FGBT) is proposed. This transistor is free of gate oxide/insulator and expected to be suitable for high temperature applications. Its static and dynamic characteristics at 300K and 600K are investigated by performing two-dimensional numerical simulations. It can be turned on with a gate voltage of 2.7V and 2.0V at 300K and 600K respectively. With a 28μm blocking layer and a horizontal channel opening of 0.15μm, this bipolar transistor is able to block over 3000V with a leakage current density smaller than 1×10⁻³ A/cm² at both 300K and 600K, and achieves a forward current density at 5V of 100 A/cm² and 134 A/cm² at 300K and 600K respectively. With a dVg/dt of 5.4×10⁵ V/s, the turn-on time is 0.23μs and the turn-off time 1.41μs at 300K. The turn-on time decreases slightly to 0.21μs and the turn-off time increases to 2.05μs at 600K.

Introduction

The commercial availability of 3-inch wafers of 4H-SiC and the continued effort in scaling up SiC substrates by a number of companies are fostering a SiC power electronic industry. A lot of 4H-SiC high voltage and high speed devices have been demonstrated with the majority of them focusing on replicating the corresponding Si power devices in the hope of achieving higher power levels, such as 5000V-100A 4H-SiC P'-i-N diode [1], 350V 6H-SiC ACCUFET with a room temperature specific on-resistance of 18mΩ.cm² at a gate voltage of 5V [2], 1400V 4H-SiC high-voltage UMOSFET with a room temperature specific on-resistance of 15.7 mΩ.cm² [3], and most recently 6,000V 4H-SiC DMOSFET [4]. It has, however, been realized that MOS-based SiC devices may not be suitable for applications under both high electric fields and high temperatures (over 150-200°C) due to the reliability concern of the gate oxide [5]. In order to take full advantage of SiC superior material properties, SiC power switches free of gate oxide/insulator need to be designed and developed. In this paper, a novel planar high voltage normally-off FGBT (see U.S. Patent 6,107,649 and other pending patents) in 4H-SiC is investigated. Normally-off power switches are preferred over normally-on devices. Normally-on power switches present substantial complication in practical applications such as power inverters for motor control. The DC and transient characteristics of this device are investigated by performing two-dimensional numerical simulations using ISE SiC TCAD module with 4H-SiC material parameters taken from the most recently published literatures.

Structure of the Normally-Off FGBT

The cross sectional view of the proposed normally-off FGBT in 4H-SiC is shown in Fig.1. The normally-off FGBT is a bipolar device. The buried N⁺ layer, which is formed by using MeV deep nitrogen implantation, is the collector. The N-type substrate is the emitter. Three P-type epilayers,
P₁ layer, P² layer and P₂ layer form the base. The implanted N⁺P gate with a length of 1µm is used to control the base current by controlling the horizontal channel opening. A semi-insulating layer formed by deep Vanadium implantation is used to terminate the horizontal channel. To keep the device normally-off, the horizontal channel is designed to be closed with intrinsic depletion when the gate voltage is zero. The normally-off FGBT cell is arranged in a simple array on the wafer. This structure has been optimized to block over 3000V by performing a large number of simulations.

**Simulations and Discussions**

In the simulations, the relationship of τₜ=5τᵣ is used. The impact ionization coefficients are taken from [6].

**Blocking Voltage.** The dependence of emitter current density (Jₑ) vs. collector-to-emitter voltage (Vₑₑ) at 300K and 600K when the device is off is shown in Fig.2. For a horizontal channel opening (Wₑₑ) of 0.18µm, the avalanche breakdown voltage increases from 3015V to 3548V and the leakage current density at Vₑₑ=3000V (hereafter termed as J₀) also increases from 6.6x10⁻⁴A/cm² to 3.8A/cm² when the temperature is increased from 300K to 600K. Two factors may account for the increase of the leakage current with temperature. One is the increase of the current gain with temperature due to the increase of the carrier lifetime with temperature. The other is that the decrease in the built-in voltage at higher temperatures causes the horizontal channel to open wider. Thus, the design of the normally-off FGBT must be performed for the highest operating temperature in order to keep the leakage current smaller than the maximum tolerable leakage current in the whole range of the operating temperature. Wₑₑ up to 0.15µm (0.18µm) ensures the J₀ to be smaller than 1x10⁻⁴A/cm² at 600K (300K), as depicted in Fig.2.

**Forward Current Density.** At zero gate bias, the horizontal channel is closed by the intrinsic depletion region. To turn on the device, a voltage must be applied to the gate to forward bias the junction between the gate N⁺ region and the drift layer P₁. The maximum allowable gate forward bias is limited by the built-in voltage of this junction and the maximum tolerable gate current density, which is set at 1A/cm² in this work. Thus, the maximum gate voltages are found to be 2.7V and 2.0V at 300K and 600K, respectively. Fig.3 shows the Jₑ-Vₑₑ curves at 300K and 600K when the device is turned fully on. For Wₑₑ equal to 0.15µm, the forward emitter current density at 5V (hereafter termed as Jₑ) reaches 100A/cm² and 134A/cm² at 300K and 600K, respectively.

**Horizontal Channel Opening.** The horizontal channel opening Wₑₑ is one of the critical parameters for the design of the normally-off FGBT as discussed earlier. The leakage current density decreases exponentially with the decrease in Wₑₑ as shown in Fig.4. At 600K, when Wₑₑ decreases from 0.18µm to 0.15µm, J₀ decreases substantially from 3.8A/cm² to 2.1x10⁻⁴A/cm². However, the forward current density also decreases from 179A/cm² to 100A/cm² at 300K and from 213A/cm² to 134 A/cm² at 600K.

**Vertical Channel Opening.** The vertical channel opening d is also one of the critical design parameters for the high voltage normally-off FGBT. It determines the avalanche breakdown voltage of the normally-off FGBT. Its effects on the avalanche breakdown voltage and Jₑ for Wₑₑ equal to 0.18µm at 300K are illustrated in Fig.5. When the vertical channel opening increases from 2µm to 3µm, the breakdown voltage decreases linearly from 3393V to 2584V while Jₑ increases from 121A/cm² to 199A/cm². The optimized value for the vertical channel opening d for a 3,000V normally-off FGBT is around 2.5µm.

**Effect of Carrier Lifetimes.** Since there is presently a large variation in the reported carrier lifetimes in 4H-SiC materials [7] although, being an indirect band gap semiconductor, its carrier lifetimes should be long, the effects of the variation of carrier lifetimes on the performance of the device have been studied and are depicted in Fig.6. The forward current density improves when electron lifetime τₑ is increased to around 2µs. Although beyond 4µs the improvement is minimum.
for this particular design, longer carrier lifetimes should make it possible to design the device with an even thicker base with improved blocking voltage capability.

**Switching Speed.** The switching speed of the normally-off FGBT is evaluated by performing transient simulations for a resistively loaded circuit with a $W_{hc}$ of 0.15μm, an emitter current density of 100A/cm², a DC bus voltage of 1,000V and a gate voltage rate of $dV_{GC}/dt$ equal to 5.4×10¹⁴V/s. The simulated switching waveforms at 300K are shown in Fig.7 where the turn-on time is found to be 0.27μs and the turn-off time 1.41μs. The switching speed is also predicted at 600K, as shown in Fig.8 where the turn-on time is found to be 0.21μs and the turn-off time 2.05μs. The turn-off time is longer at 600K than at 300K because the carrier lifetimes in 4H-SiC increase with temperature, a longer time is needed to remove the excess carriers stored in base during turn-off. The turn-on time is a little bit shorter at 600K than at 300K because the increase of the current gain can speed up the building-up of the electrons in the base which reduces the turn-on time. The above results show that the normally-off FGBT is able to switch a drain current density of 100A/cm² at a few hundred kHz range at both 300K and 600K.
Summary

The proposed 3,000V 4H-SiC normally-off FGBT has been studied by two-dimensional numerical simulations. Being free of gate oxide/insulator, this structure is suitable for very high temperature applications. For applications at near room temperature, a horizontal channel opening up to 0.18µm can be used with a leakage current density of $6.6\times10^4$A/cm² at $V_{CE}=3000$V in off state and a forward current density of 179A/cm² at $V_{CE}=5$V. For applications up to 600K, a horizontal channel opening up to 0.15µm can be used with a leakage current density of $2.1\times10^4$A/cm² at $V_{CE}=3000$V in off state and a forward current density of 134A/cm² at $V_{CE}=5$V. High quality wafers of 4H-SiC with electron lifetime greater than 2µs are desirable for fabricating this 3,000V normally-off FGBT. The optimal vertical channel opening is around 2.5µm. With a gate voltage rate of $dV_{GE}/dt$ equal to $5.4\times10^3$V/s, the 4H-SiC normally-off FGBT is able to switch a drain current density of 100A/cm² at a few hundred kHz range at both 300K and 600K. Further optimization work is under way and the feasibility fabrication results will be reported later.

References