Rutgers University, Department of Electrical and Computer Engineering
ABET COURSE SYLLABUS
COURSE: 14:332:437

Course Catalog Description: 14:332:437 -- Digital Systems Design (3)
Hardware description using the Verilog language. Design methodologies
for combinational and sequential logic circuits. Characteristics of
microprocessors, fault-tolerant computer design, computer arithmetic, and
advanced state machine theory. Digital machine organization for testing
and fault-tolerance.

Pre-Requisite Courses: 14:332:231, 252, 331

Co-Requisite Courses: None

Pre-Requisite by Topic:
1. Digital Logic Design
2. Flip-flop and State Machine Design
3. Programming Methodology
4. Computer Architecture

Textbook & Materials:
P. Lala, Self-Checking and Fault-Tolerant Digital Design, Morgan Kaufmann

D. Thomas and P. Moorby, The Verilog Hardware Description Language, 5th

M. Bushnell and V. Agarwal, Essentials of Electronic Testing for Digital

Overall Educational Objective: To prepare students for the design of practical digital hardware systems
using Verilog.

Course Learning Outcomes: A student who successfully fulfills the course requirements will have
demonstrated:
1. An ability to describe and design computer hardware using the Verilog
hardware description language.
2. An ability to rapidly design combinational and sequential logic that
works.
3. An ability to rapidly design complex state machines (present in all
practical computers) that work.
4. An ability to design logic and state machines using an Automatic
Logic Synthesis program.
5. An ability to implement state machines using Field-Programmable
Gate Arrays.
6. An ability to design high-speed computer arithmetic circuits.
7. An ability to design a computer to be fault-tolerant.
8. An ability to design a computer memory using error-correcting codes.
9. An ability to design a computer so that it can test itself with built-in
circuitry.
How Course Outcomes are Assessed:
Homeworks (10): 12.5%
Practicum Exams (4): 12.5%
Two Mid-Term Exams: 45%
Final Exam: 30%

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<tr>
<th>Outcome</th>
<th>Level</th>
<th>Proficiency assessed by</th>
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<tbody>
<tr>
<td>(a) an ability to apply knowledge of Mathematics, science, and engineering</td>
<td>H</td>
<td>HW Problems, Exams</td>
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<td>(b) an ability to design and conduct experiments and interpret data</td>
<td>S</td>
<td>Design Problems in HW and Exams</td>
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<td>(c) an ability to design a system, component or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability</td>
<td>N</td>
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<td>(d) an ability to function as part of a multi-disciplinary team</td>
<td>N</td>
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<td>(e) an ability to identify, formulate, and solve ECE problems</td>
<td>H</td>
<td>HW Problems, Exams</td>
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<td>(f) an understanding of professional and ethical responsibility</td>
<td>N</td>
<td></td>
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<td>(g) an ability to communicate in written and oral form</td>
<td>S</td>
<td>HW Problems</td>
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<td>(h) the broad education necessary to understand the impact of electrical and computer engineering solutions in a global, economic, environmental, and societal context</td>
<td>N</td>
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<td>(i) a recognition of the need for, and an ability to engage in life-long learning</td>
<td>S</td>
<td>Home-work, discussions during lectures</td>
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<td>(j) a knowledge of contemporary issues</td>
<td>N</td>
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<tr>
<td>Basic disciplines in Electrical Engineering</td>
<td>S</td>
<td>HW Problems, Exams</td>
</tr>
<tr>
<td>Depth in Electrical Engineering</td>
<td>S</td>
<td>HW Problems, Exams</td>
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<tr>
<td>Basic disciplines in Computer Engineering</td>
<td>H</td>
<td>P-Spice Simulations</td>
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<tr>
<td>Depth in Computer Engineering</td>
<td>H</td>
<td></td>
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<tr>
<td>Laboratory equipment and software tools</td>
<td>S</td>
<td>HW Problems, Mid-Term Exams</td>
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<td>Variety of instruction formats</td>
<td>S</td>
<td>Lecture, office hour discussions</td>
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Topics Covered Week by Week:
Week 1: Fault Tolerance Fundamentals and Triple Modular Redundancy
Week 2: Advanced Combinational Logic Design
Week 3: Verilog Language - Standard Combinational Logic
Week 4: Verilog Language - Concurrency and Sequential Logic
Week 5: Verilog Language - Tri-State Logic, Examples
Week 6: State Machines – Timing Analysis, False Paths, Counters
Week 7: State Machines – Synthesis to Handle Timing Delays, Asynchronous Inputs
Week 8: Exam I, State Machine Synchronizers
Week 9: Fault Tolerance -- Time and Information Redundancy
Week 10: Fault Tolerance -- Parity, Arithmetic, Cyclic and Hamming Codes
Week 11: Computer Arithmetic, Wallace Tree Multipliers and Dividers
Week 12: Testing, Fault Modeling and Test Generation , Hourly Exam II
Week 13: Built-In Self-Testing, Design for Testability
Week 14: Packaging and Rapid Prototyping – Microprocessor Design
Week 15: Final Examination

Computer Usage: Students use the Synopsys Design_Analyzer tool to synthesize hardware from Verilog hardware descriptions, and the Synopsys vcs behavioral/logic simulator to simulate the Verilog descriptions.

Laboratory Experiences: There are 10 Homework assignments that require students to use the circuit design software in the laboratory.

Design Experiences: The 10 Homework assignments are all hardware design experiences.

Independent Learning Experiences: The 10 Homework assignments.
Contribution to the Professional Component:
(a) College-level Mathematics and Basic Sciences: 0.0 credit hours
(b) Engineering Topics (Science and/or Design): 3.0 credit hours
(c) General Education: 0.0 credit hours
Total credits: 3

Prepared by: M. Bushnell
Date: September 2007