Rutgers, The State University of New Jersey
College of Engineering, Department of Electrical and Computer Engineering

16:332:599 Advanced Topics in Solid-State Electronics (3)
Spring 2012
Tuesdays, 5:00 p.m. – 8:00 p.m., EE 240

Instructor	Jaeseok (“Jae”) Jeon, jaeseok.jeon *at* rutgers *dot* edu EE 122 (temporary), EE 217
Office Hours	T.B.A.
Brief Course Description	16:332:599 Advanced Topics in Solid-State Electronics (3): Overview of basic MOSFET theory and issues; advanced MOSFET physics; advanced transistor structures; emerging research devices and applications
Course Objective	To understand the technical challenges of scaled bulk MOSFETs and learn about the advanced transistor structures adapted to overcome the issues, and hence, learn the skills needed to design and analyze new devices yet to be invented
Prerequisite	16:332:583 Semiconductor Devices I (3) or 14:332:465 Physical Electronics (3) or *Equivalent* Students who lack the prerequisite must contact the instructor.
Primary Text	• Y. Taur & T. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998. **(on 2-hour reserve at Science and Engineering Reading Center)**
Reference Texts	• S. Wolf, *The Submicron MOSFET, vol. 3 of Silicon Processing for the VLSI Era*, Lattice Press, 1995. • R. S. Muller & T. I. Kamins, *Device Electronics for Integrated Circuits, 3rd Ed.*, John Wiley & Sons, Inc., 2003. **(on 2-hour reserve at Science and Engineering Reading Center)** • B. L. Anderson & R. L. Anderson, *Fundamentals of Semiconductor Devices*, McGraw-Hill, 2005. • R. F. Pierret, *Semiconductor Device Fundamentals*, Addison-Wesley, 1996. **(on 2-hour reserve at Science and Engineering Reading Center)** • B. G. Streetman & S. K. Banerjee, *Solid State Electronic Devices, 6th Ed.*, Pearson/Prentice Hall, 2006. **(on 2-hour reserve at Science and Engineering Reading Center)**
Grading Policy	Homework: 20 % Midterm and final exams: 80 %
Exams	All exams are cumulative, open books, and open notes; Make-up exams will be allowed only under special circumstances.
Policy on Academic Dishonesty	**http://academicintegrity.rutgers.edu/integrity.shtml**

(Tentative) Lecture Schedule

1. <u>**Overview of Basic MOSFET (2 Weeks)**</u>

   1.1. Threshold Voltage (V_{TH}) Issues
   V_{TH} and body effect; effects of retrograde body doping ion implantation, and non-uniform doping on V_{TH}

   1.2. Basic MOSFET Theory
   Channel length modulation (CLM); ideal *I-V* characteristic; square law, including body effect; drain saturation voltage; saturation current (I_{DSAT}) and transconductance (g_m); bulk charge theory; charge sheet model; subthreshold current; subthreshold swing; subthreshold slope; gain-induced drain leakage (GIDL)

2. <u>**Advanced MOSFET Physics (5 Weeks)**</u>

   2.1. *Off*-State Characteristics of Scaled MOSFETs
   MOSFET scaling theory; short-channel effect (SCE); drain-induced barrier lowering (DIBL); effect of body-bias on short-channel effect; narrow width effect; reverse short channel effect; sub-surface punch-through

   2.2. *On*-State Characteristics of Scaled MOSFETs
   Mobility measurement; mobility dependency; scattering effects; universal mobility curve; universal surface motility; velocity saturation; square law model *vs.* improved velocity saturation model; parasitic source-drain resistance; source injection velocity limit; channel length modulation (CLM); output resistance; MOSFET device design; surface- *vs.* buried-channel PMOS; latch-up

   2.3. Hot-Carrier Effect
   Hot electron effect; lightly-doped drain (LDD); substrate current; device lifetime; PMOS hot electron effect; oxide interface improvement

   2.4. Gate Stack Engineering (Gate Oxides and Electrodes)
   Conduction in insulators; tunneling currents; dielectric reliability; oxide breakdown; hole generation / trapping model; oxide leakage; gate stack scaling; high-K dielectrics (overview, issues, materials, and requirements); materials and requirements for gate electrodes; work function engineering

3. <u>**Advanced Transistor Structures (5 Weeks)**</u>

   3.1. Brief Overview of Modern MOSFET Fabrication Process, Including Intel's 45 nm High-K Technology

   3.2. Solutions to the Issues with Scaled Bulk MOSFETs

   3.2.1. Series Resistance: Raised source/drain MOSFET; Schottky source/drain

   3.2.2. Mobility: Strained silicon (technologies, device characteristics, process integration issues, junction leakage, and strain relaxation); velocity saturation; high field transport; channel engineering

   3.2.3 Leakage: Silicon-On-Insulator (SOI) (technologies, challenges, device characteristics, fully-depleted *vs.* partially-depleted); ultra-thin-body (UTB) MOSFETs

   3.3. Sources and Impacts of MOSFET Variation
   V_{TH} variation; random dopant fluctuation (RDF); line edge roughness (LER); random telegraph noise (RTN)

   3.4. Multi-Gate MOSFETs: *The* "FinFETs," which is "the *only* transistor design picked up by the industry."

   3.5. (Optional) Memory Technology Overview
   SRAM; DRAM; Flash Memory (NAND *vs.* NOR)

4. <u>**Emerging Research Devices and Applications (3 Weeks)**</u>

   4.1. To Enable Ultimately-Scaled Transistors
   Nanowire (NW) FETs; Carbon-Nano-Tube (CNT) FETs

   4.2. To Achieve Very-Low-Power Consumption
   Tunneling-FETs (TFETs); Nano-Electro-Mechanical (NEM) Relays; Ferroelectric Transistors

   4.3. (Optional) To Realize Denser, Faster, and Lower-Power Memory than Flash
   Resistive-RAM (RRAM); Phase Change Memory (PCM)