Rutgers, The State University of New Jersey
College of Engineering, Department of Electrical and Computer Engineering

Semiconductor Devices I
16:332:583 Spring 2013

Lectures: Tuesday, 06:40 - 09:20 p.m. in SEC-211

Instructor	Jaeseok ("Jae") Jeon EE 217, jjeon@ece.rutgers.edu
Office Hours	By appointment
Course Catalog Description	16:332:583 Semiconductor Devices I (3): Charge transport, diffusion and drift current, injection, lifetime, recombination and generation processes, P-N junction devices, transient behavior, FET's, *I-V*, and frequency characteristics, MOS devices *C-V*, *C-f*, and *I-V* characteristics, operation of bipolar transistors.
Prerequisite	14:332:465 Physical Electronics (3); Students who lack the prerequisite must contact the instructor.
Primary Text	• Y. Taur & T. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998.
Reference Texts	• S. Wolf, *Chapters 3, 4, 5, & 9 of The Submicron MOSFET, vol. 3 of Silicon Processing for the VLSI Era*, Lattice Press, 1995. • R. F. Pierret, *Semiconductor Device Fundamentals*, Addison-Wesley, 1996. • B. G. Streetman & S. K. Banerjee, *Solid State Electronic Devices, 6th Ed.*, Pearson/Prentice Hall, 2006. • C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, Pearson/Prentice Hall, 2010. • B. L. Anderson & R. L. Anderson, *Fundamentals of Semiconductor Devices*, McGraw-Hill, 2005. • R. S. Muller & T. I. Kamins, *Device Electronics for Integrated Circuits, 3rd Ed.*, John Wiley & Sons, Inc., 2003.
Grading Policy	3 homework assignments: 20 % 1 mid-term and 1 final exams: 80 %
Homework	Homework assignments will be given every month and must be turned in on their due dates to count for full credit. Grades will be reduced by 10 % for each "school day" late. You are encouraged to discuss the homework with your class mates, however, direct copying of another student's work is not allowed. Please feel free to contact the instructor via email or during the office hours for clarifications and hints for the homework problems.
Exams	All exams are cumulative, closed books; Make-up exams will be allowed only under special circumstances.
Policy on Academic Dishonesty	**http://academicintegrity.rutgers.edu/integrity.shtml**

Course Objective

- To develop a physical understanding of deep sub-micron (as well as long-channel) charge-based, current- and post-CMOS transistors.

- To learn the general skills for analyzing and designing semiconductor devices and explore future new devices yet to be invented.

(Tentative) Lecture Schedule

1. **Overview of Basic MOSFET (2 Weeks)**

   1.1. Threshold Voltage (V_{TH}) Issues
   V_{TH} and body effect; effects of retrograde body doping ion implantation, and non-uniform doping on V_{TH}

   1.2. Basic MOSFET Theory
   Channel length modulation (CLM); ideal *I-V* characteristic; square law, including body effect; drain saturation voltage; saturation current (I_{DSAT}) and transconductance (g_m); bulk charge theory; charge sheet model; subthreshold current; subthreshold swing; subthreshold slope; gain-induced drain leakage (GIDL)

2. **Advanced MOSFET Physics (5 Weeks)**

   2.1. *Off*-State Characteristics of Scaled MOSFETs
   MOSFET scaling theory; short-channel effect (SCE); drain-induced barrier lowering (DIBL); effect of body-bias on short-channel effect; narrow width effect; reverse short channel effect; sub-surface punch-through

   2.2. *On*-State Characteristics of Scaled MOSFETs
   Mobility measurement; mobility dependency; scattering effects; universal mobility curve; universal surface motility; velocity saturation; square law model *vs.* improved velocity saturation model; parasitic source-drain resistance; source injection velocity limit; channel length modulation (CLM); output resistance; MOSFET device design; surface- *vs.* buried-channel PMOS; latch-up

   2.3. Hot-Carrier Effect
   Hot electron effect; lightly-doped drain (LDD); substrate current; device lifetime; PMOS hot electron effect; oxide interface improvement

   2.4. Gate Stack Engineering (Gate Oxides and Electrodes)
   Conduction in insulators; tunneling currents; dielectric reliability; oxide breakdown; hole generation / trapping model; oxide leakage; gate stack scaling; high-K dielectrics (overview, issues, materials, and requirements); materials and requirements for gate electrodes; work function engineering

3. **Advanced Transistor Structures (5 Weeks)**

   3.1. Brief Overview of Modern MOSFET Fabrication Process, Including Intel's 45 nm High-K Technology

   3.2. Solutions to the Issues with Scaled Bulk MOSFETs

   3.2.1. Series Resistance: Raised source/drain MOSFET; Schottky source/drain

   3.2.2. Mobility: Strained silicon (technologies, device characteristics, process integration issues, junction leakage, and strain relaxation); velocity saturation; high field transport; channel engineering

   3.2.3 Leakage: Silicon-On-Insulator (SOI) (technologies, challenges, device characteristics, fully-depleted *vs.* partially-depleted); ultra-thin-body (UTB) MOSFETs

   3.3. Sources and Impacts of MOSFET Variation
   V_{TH} variation; random dopant fluctuation (RDF); line edge roughness (LER); random telegraph noise (RTN)

   3.4. Multi-Gate MOSFETs: *The* "FinFETs," which is "the *only* transistor design picked up by the industry."

   3.5. (Optional) Memory Technology Overview: SRAM; DRAM; Flash Memory (NAND *vs.* NOR)

4. **Emerging Research Devices and Applications (3 Weeks)**

   4.1. To Enable Ultimately-Scaled Transistors
   Nanowire (NW) FETs; Carbon-Nano-Tube (CNT) FETs

   4.2. To Achieve Very-Low-Power Consumption
   Tunneling-FETs (TFETs); Nano-Electro-Mechanical (NEM) Relays; Ferroelectric Transistors

   4.3. (Optional) To Realize Denser, Faster, and Lower-Power Memory than Flash:
   Resistive-RAM (RRAM); Phase Change Memory (PCM)