ECE Capstone program
Spring 2019
Project Abstract & Info

Please provide the following information to be shared with on capstone information exchange platform:

1. Project number: S19-46

2. Project title (as will appear on the poster): RISC-V Processor & Applications on FPGA

3. Team members:
Oz Bejerano
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Alex Riveron
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4. Adviser(s) name(s):
Professor Phil Southard
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5. Up to 5 keywords that will help to classify the project scope:
RISC-V
Embedded
FPGA
Computer
Processor

6. Project abstract (up to 250 words) to be shared with judges:

Our group has implemented a RISC-V processor on a FPGA. The implementation is a system comprised of a RISC-V processor with an interactive terminal interface. The processor is a single-core, pipelined, 32-bit RV32I processor, which includes the base instruction set "I". The processor contains a full single issue, in-order five stage pipeline with hazard detection. Pipelining splits the processor into 5 stages, each with a different purpose: fetching an instruction, decoding the instruction, executing the instruction, accessing memory, and storing instruction output to a register. The pipeline allows the processor to compute 5 instructions in different stages of execution on the same clock cycle. This processor is written in VHDL and is RISC-V compliant.

We have included a suite of additional features and software to showcase some of the possible applications of our processor. To interact with the processor, we have implemented a terminal interface on a VGA display that enables users to run programs as a demonstration of some of its capabilities. These programs accept user input from interfaces on the FPGA board and display output to the user, show graphics using ASCII text, and even run small games utilizing the terminal. This project has been featured as an entry into the Harris Corporation 2019 Senior Project Mentor Program, and we have received guidance from industry experts on how to design and implement our project.