## Configurable In-line Video Refinement (CIVR)

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### Motivations and Objectives

#### Motivations

- Many modern graphics processing algorithms involve full-frame analysis and computation which requires high-overhead computations prior to displaying the display output causing lag
- Existing external boxes usually only implement a single feature each and would be extremely costly to implement all of our features

#### Objectives

- Create a low latency inexpensive video refinement unit
- Incorporate many common graphics enhancements (anti-aliasing, dithering, etc.)

### Research Challenges

- DVI shield and mounting holes not to spec due to error in Molex datasheet
- Blue and green output noise due to the most significant bit data lines being too long and not arriving in time for the positive edge of pixel clock
- JTAG programmer would not detect the FPGA
- Level-shifting MOSFETs are too slow to communicate via I2C at 100 kbps to transmit and modify EDID

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### References

1. [Max 10 Documentation](https://www.altera.com/products/fpga/max-series/max-10/support.html)