Michael L. Bushnell, Professor I

Years Service at Rutgers: 20 years
1986 – Assistant Professor; 1992 – Associate Professor; 1999 - Professor

Degrees:
Ph.D. in Electrical Engineering, Carnegie Mellon University, 1986.
M.S. in Computer Engineering, Carnegie Mellon University, 1983.
S.B. in Electrical Engineering and Computer Science, MIT, 1975.

Other Related Experience (teaching, industrial, etc.):
1979 – 1981 Applicon, Inc.; Member of Technical Staff.
1976 – 1979 Instron Corporation, Canton, MA; Senior Systems Programmer.
1974 – 1976 Honeywell Information Systems, Billerica, MA; Associate Engineer.

Consulting, Patents, etc.:

- B. Yu and M. L. Bushnell, "A Novel Dynamic Power Cutoff Technique (DPCT) for Active Leakage Reduction in Deep Submicron CMOS Circuits," U.S. Provisional Patent, Filed Oct. 2006.
- H. Venkatanarayanan and M. L. Bushnell, "An Area Efficient Mixed-Signal Test Architecture for Systems-on-a-Chip," U. S. Provisional Patent, Filed Jan. 1, 2006.
- L. Rao, and M. L. Bushnell, "Graphical IDDQ Signatures for ULSI Testing," U. S. Patent # 6,812,724 B2, Issued Nov. 2, 2004.
- L. Rao and M. L. Bushnell , "Graphical IDDQ Signatures for ULSI Testing," International Patent Application # PCT/US03/05582, International Publication # WO 03/073114 A1, Pending, Filed Sept. 11, 2003.
- R. Ramadoss and M. L. Bushnell, "Test Generation for Analog Circuits Using Partitioning and Inverted System Simulation," U. S. Patent # 6,308,300 B1, Issued Oct. 23, 2001.
- M. L. Bushnell and G. Parthasarathy, "Method and Apparatus for Combined Stuck-at Fault and Partial-Scanned Delay-fault Built-In Self-Test," U. S. Patent # 6,247,154 B1, Issued Jun. 12, 2001.
- M. A. Gharaybeh, M. L. Bushnell, and V. D. Agrawal, "Method and System for Identifying Tested Path Delay Faults," U. S. Patent # 6,131,181, Issued Oct. 10, 2000.
- M. L. Bushnell and I. Shaik , "Robust Delay Fault Built-In Self-Testing Method and Apparatus," Verfahren und Vorrichtung zur Robusten und Automatischen Prüfung von Verzögerungsfehlern, Procede et Apparei de Test Automatique Intgegre D'Anomalie de Retard Dans un Materiel, European Patent # EP 0 663 092 B1, Filed 7/21/1994, Issued March 22, 2000.
- R. Ramadoss and M. L. Bushnell , "Test Generation for Mixed-Signal Devices Using Signal Flow Graphs," U.S. Patent # 5,831,437, Issued Nov. 3, 1998.
- M. L. Bushnell and I. P. Shaik, "Robust Delay Fault Built-In Self-Testing Method and Apparatus," U.S. Patent # 5,422,891, Issued June 6, 1995.

Principal Publications (last five years):

- B. Yu and M. L. Bushnell, "A Novel Dynamic Power Cutoff Technique (DPCT) for Active Leakage Reduction in Deep Submicron CMOS Circuits," *Int'l. Symp. on Low-Power Electronics and Design*, Oct. 2006, pp 214-219.
- R. Sethuram, S. Wang, S. T. Chakradhar, and M. L. Bushnell, "Zero Cost Test Point Insertion Technique for Structured ASICs," *VLSI Design 2007*, Jan. 2007.
- S. K. Devanathan and M. L. Bushnell, "Test Pattern Generation Using Modulation by Haar Wavelets and Correlation for Sequential BIST," *VLSI Design 2007*, Jan. 2007.

- J. Ayres, and M. L. Bushnell, “Analog Circuit Testing Using Auto Regressive Moving Average (ARMA) Models,” *VLSI Design 2007*, Jan. 2007.
- R. Pandey, and M. L. Bushnell, “Architecture for Variable-Length Combined FFT, DCT, and MWT Transform Hardware for a Multi-Mode Wireless System,” *VLSI Design 2007*, Jan. 2007.
- D. Mazor, M. L. Bushnell, D. J. Mulligan, and R. J. Blaikie, “Fault Models and Device Yield of a Large Population of Room Temperature Operation Single-Electron Transistors,” *VLSI Design 2007*, Jan. 2007.
- R. Sethuram, H. Venkatanarayanan, O. Khan, and M. L. Bushnell, “Power Reduction Using a Novel Neural Net Branch Predictor,” *VLSI Design 2007*, Jan. 2007.
- T. Raja, V. D. Agrawal, and M. L. Bushnell, “Transistor Sizing of Logic Gates to Maximize Input Delay Variability,” *JOLPE -- J. of Low Power Electronics*, accepted, 2006.
- H. V. Venkatanarayanan and M. L. Bushnell, "An Area Efficient Mixed-Signal Test Architecture for Systems-on-a-Chip," *VLSI Design 2006*, pp. 161-168, 2006.
- S. K. Devanathan and M. L. Bushnell, "Sequential Spectral ATPG Using the Wavelet Transform and Compaction," *VLSI Design 2006*, pp. 407-412, 2006.
- S. Chary and M. L. Bushnell, "Automatic Path-Delay Fault Test Generation for Combined Resistive Vias, Resistive Bridges, and Capacitive Crosstalk Delay Faults," *VLSI Design 2006*, pp. 413-418, 2006.
- O. Khan, M. L. Bushnell, "Aliasing Analysis of Spectral Statistical Response Compaction Techniques,” *VLSI Design 2006,"* pp. 801-806, 2006.

Scientific and Professional Society Memberships:
- Member, Institute of Electrical and Electronic Engineers (IEEE) – Computer Society, Circuits
- and Systems Society, Engineering Management Society
- Member, Association for Computing Machinery (ACM) – Special Interest Groups for Design Automation, Computer Graphics, Artificial Intelligence
- Member, VLSI Society of India (VSI)

Honors and Awards:
- N. N. Biswas Best Student Paper Prize, “An Area Efficient Mixed-Signal Test Architecture for Systems-on-a-Chip,” Int’l. Conf. on VLSI Design, Jan. 2006, H. Venkatanarayanan and M. Bushnell.
- Best Student Paper Prize, “New Graphical IDDQ Signatures Reduce Defect and Yield Loss,” North Atlantic Test Workshop, May 2002, L Rao, M. L. Bushnell and V. D. Agrawal.
- M. L. Bushnell assisted his students, G. Parthasarathy and M. Iyer to design the Prize VLSI Chip (A Branch Prediction Controller for a RISC Processor) that uses Built-In Self-Test and Boundary Scan. This was judged the best novice chip design in the United States in the 1996 Mentor Graphics National Chip Design competition.

Institutional and Professional Service (last five years):
- Member, New Brunswick Computing Advisory and Information Sciences Committees
- Member, University Transportation Coordinating Council
- Member, ECE Department Undergraduate Curriculum Committee
- Technical Program Committee Co-Chairman, 19th Int’l. Conf. on VLSI Design, Jan. 2006, India.

Professional Development Activities (last five years):
- Developed the senior elective concepts and design course sequences-
- 14:332:437, 438 Capstone Design – Digital Systems
- 14:332:479, 480 Capstone Design – VLSI

- Wrote the leading circuit testing textbook, *Essentials of Electronic Testing for Digital, Memory, and Mixed-Signal VLSI Circuits*, Springer, 2000, used by more than 80 Universities, with V. D. Agrawal.