Rutgers University, Department of Electrical and Computer Engineering
ABET COURSE SYLLABUS
COURSE: 14:332:479

Course Catalog Description: 14:332:479 VLSI Design (3)
Introductory digital VLSI chip design. CMOS technology, dynamic clocked logic, layout design rules, and analog MOSFET timing analysis. Computer-aided design software tools and elementary circuit testing. Cell library construction.

Pre-requisite Courses: 14:332:231, 331, 366

Co-Requisite Courses: None

Pre-Requisite by Topic:

1. Digital Logic Design
2. Computer Architecture and Assembly Language
3. Digital Electronics

Textbook & Materials: N. Weste and D. Harris, *Principles of CMOS VLSI Design: A Systems Perspective,* 3rd Ed., Addison-Wesley, 2005.

M. Bushnell and V. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*, Springer, 2000 (optional).

Overall Educational Objective: To introduce students to basic concepts of digital VLSI chip design.

Course Learning Outcomes: A student who successfully fulfills the course requirements will have demonstrated:

1. An ability to design logic circuit layouts for both static CMOS and dynamic clocked CMOS circuits.
2. An ability to extract the analog parasitic elements from the layout and analyze the circuit timing using a logic simulator and an analog simulator.
3. An ability to build a cell library to be used by other chip designers.
4. An ability to insert elementary testing hardware into the VLSI chip.
5. An ability to analyze VLSI circuit timing using Logic Effort.
6. An ability to design elementary data paths for microprocessors, including moderate-speed adders, subtracters, and multipliers.
7. An ability to estimate and compute the power consumption of a VLSI chip.
8. An ability to assemble an entire chip and add the appropriate pads to a layout
9. An ability to explain the chip technology scaling process.

How Course Outcomes are Assessed:
Homeworks (10): 40%
Mid-Term Exam: 30%
Final Exam: 30%
Total: 100%

N = none S = Supportive H = highly related

Outcome	Level	Proficiency assessed by
(a) an ability to apply knowledge of Mathematics, science, and engineering	H	HW Problems, Exams
(b) an ability to design and conduct experiments and interpret data	H	Design Problems in HW and Exams
(c) an ability to design a system, component or process to meet desired needs within realistic constraints such as economic, environmental, social, political,	N	

ethical, health and safety, manufacturability, and sustainability		
(d) an ability to function as part of a multi-disciplinary team	N	
(e) an ability to identify, formulate, and solve ECE problems	H	HW Problems, Exams
(f) an understanding of professional and ethical responsibility	N	
(g) an ability to communicate in written and oral form	S	HW Problems
(h) the broad education necessary to understand the impact of electrical and computer engineering solutions in a global, economic, environmental, and societal context	N	
(i) a recognition of the need for, and an ability to engage in life-long learning	H	Home-work, discussions during lectures
(j) a knowledge of contemporary issues	N	
(k) an ability to use the techniques, skills, and modern engineering tools necessary for electrical and computer engineering practice	H	HW Problems, Exams
Basic disciplines in Electrical Engineering	H	HW Problems, Exams
Depth in Electrical Engineering	H	HW Problems, Exams
Basic disciplines in Computer Engineering	H	P-Spice Simulations
Depth in Computer Engineering	H	
Laboratory equipment and software tools	H	HW Problems, Mid-Term Exams
Variety of instruction formats	S	Lecture, office hour discussions

Topics Covered Week by Week:

Week 1: Overview of VLSI and ULSI Technology, Automatic chip layout, Analog circuit simulation for digital circuit design, Structured design methodologies
Week 2: CMOS Processing Technology, logic gate, MUX, and D flip-flop design.
Week 3: MIPS Microprocessor example
Week 4: MOS Transistor Theory and Models for Resistance and Capacitance calculation
Week 5: Logical Effort
Week 6: Combinational circuits and CMOS logic families
Week 7: Sequential circuits and layout
Week 8: Analog simulation and Adder design
Week 9: Data path design and SRAM design
Week 10: Midterm and VLSI circuit testing
Week 11: VLSI circuit built-in self-testing
Week 12: Boundary scan standard and circuit reliability
Week 13: Power estimation and chip packaging
Week 14: Pads and scaling
Week 15: Case study of Intel microprocessors and Final Examination

Computer Usage: Extensive use of CAD software (from Synopsys and Cadence) to synthesize hardware, lay out VLSI circuits, and simulate circuit timing.

Laboratory Experiences: Extensive synthesis and simulation-based small computer projects in the Homework.

Design Experiences: Extensive synthesis and simulation-based computer projects, where the student can explore design alternatives.

Independent Learning Experiences: The Homework assignments.

Contribution to the Professional Component:

(a) College-level Mathematics and Basic Sciences: 0.0 credit hours
(b) Engineering Topics (Science and/or Design): 3.0 credit hours
(c) General Education: 0.0 credit hours
Total credits: 3

Prepared by: M. L. Bushnell
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