Rutgers University, Department of Electrical and Computer Engineering

ABET COURSE SYLLABUS

COURSE: 14:332:231

Course Catalog Description: 14:332:231 - Digital Logic Design (3)
Binary arithmetic, Boolean algebra, K-maps, Combinational circuit synthesis, Combinational MSI circuits, Sequential logic, Synchronous state machine design, Sequential MSI circuits.

Pre-Requisite Course: 01:440:127

Co-Requisite Courses: 01:640:251 and 14:332:233

Pre-Requisite by Topic:
1. Boolean algebra.
2. Electrical concepts from physics.
3. General computer skills.

Textbook & Materials: J.F. Wakerly: Digital Design Principles & Practices, 4th Ed., Prentice Hall, 2004; class and recitation notes.

References: The OneKey access from Prentice Hall can be helpful to solve the homework problems.

Overall Educational Objective: To introduce the basic tools for design with combinational and sequential digital logic and state machines. To learn simple digital circuits in preparation for computer engineering.

Course Learning Outcomes: A student who successfully fulfills the course requirements will have demonstrated:

1. An ability to define different number systems, binary addition and subtraction, 2's complement representation and operations with this representation.
2. An ability to understand the different switching algebra theorems and apply them for logic functions.
3. An ability to define the Karnaugh map for a few variables and perform an algorithmic reduction of logic functions.
4. An ability to define the following combinational circuits: buses, encoders/decoders, (de)multiplexers, exclusive-ORs, comparators, arithmetic-logic units; and to be able to build simple applications.
5. An ability to understand the bistable element and the different latches and flip-flops.
6. An ability to derive the state-machine analysis or synthesis and to perform simple projects with a few flip-flops.
7. An ability to understand sequential circuits, like counters and shift registers, and to perform simple projects with them.

How Course Outcomes are Assessed: Homework problems are not collected (0%)
Two midterm exams (30% + 30%)
Final exam (40%)

N = none **S = Supportive** **H = highly related**

Outcome	Level	Proficiency assessed by
(a) an ability to apply knowledge of mathematics, science, and engineering	H	R/HW problems, exams
(b) an ability to design and conduct experiments and interpret data	H	Design problems in R/HW, exams
(c) an ability to design a system, component or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability	S	Design problems in R
(d) an ability to function as part of a multi-disciplinary team	N	
(e) an ability to identify, formulate, and solve ECE problems	H	R/HW problems, exams
(f) an understanding of professional and ethical responsibility	S	HW, exams
(g) an ability to communicate in written and oral form	S	R, exams
(h) the broad education necessary to understand the impact of electrical and computer engineering solutions in a global, economic, environmental, and societal context	N	
(i) a recognition of the need for, and an ability to engage in life-long learning	S	R/HW, discussions during lectures
(j) a knowledge of contemporary issues	N	
(k) an ability to use the techniques, skills, and modern engineering tools necessary for electrical and computer engineering practice	H	R/HW problems, exams
Basic disciplines in Electrical Engineering	S	In the lectures
Depth in Electrical Engineering	S	In the lectures
Basic disciplines in Computer Engineering	H	R/HW problems, exams
Depth in Computer Engineering	H	R/HW problems, exams
Laboratory equipment and software tools	H	R problems
Variety of instruction formats	S	Lecture, office hour discussions

R = recitation HW = homework

Topics Covered Week by Week:

Week 1: Organizational issues. Information revolution. Basic hardware concepts.

Week 2: Number systems, Binary addition, subtraction, Representation of negative numbers, 2's complement addition/subtraction.

Week 3: Switching algebra, Theorems, Standard representation of logic functions.

Week 4: Combinational circuits, Truth table, Karnaugh maps, Minimization techniques.

Week 5: "Don't care" inputs, Five variable Karnaugh maps, Timing hazards.

Week 6: Documentation standards, Input/output circuits, Buses. TEST I.

Week 7: Encoders/Decoders. MUX/DMUX/XOR circuits.

Week 8: Comparators. Design examples with MSI. ALU and PLD circuits.

Week 9: Bistable elements. Latches and Flip-flops.

Week 10: State-machine design analysis and synthesis.

Week 11: State machine design examples. TEST II.

Week 12: Transition lists and ASM charts, Sequential MSI circuits, Switch debouncing.

Week 13: Counters: serial and parallel, Design examples, Shift registers.

Week 14: Design of a one-lane traffic controller, Review.

Weeks 15 and 16: Final exam.

Computer Usage: At present time the students are not using a computer. If a *simple* digital logic design program will become available, the laboratory will be redesigned accordingly.

Laboratory Experiences: It is a separate course, 14:332:233, associated with this course.

Design Experiences: A lot of the homework problems are in fact designing small circuits.

Independent Learning Experiences: Homeworks. The three exams.
Contribution to the Professional Component:

(a) College-level mathematics and basic sciences: 0.25 credit hours
(b) Engineering Topics (Science and/or Design): 2.75 credit hours
(c) General Education: 0 credit hours

Total credits: 3

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Date: July 2007